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Design and testing of a novel single-stage half-bridge AC-DC converter for battery charging

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AC-DC converters are used in most of the electrical utility applications especially in battery charging. Here, a novel topology for single-stage bridgeless AC-DC converter is presented which can give an isolated output voltage and input power factor correction. The input current to an AC-DC converter is rich in low order harmonics and so the total harmonic distortion is high and input power factor is poor. Hence Power Factor Correction (PFC) schemes have been implemented. The effectiveness of the converter is tested and verified in PSIM™ simulation software and in experimental hardware prototype. This topology is found to have reduced losses and better power factor correction compared to the single-stage PFC AC to DC converters with full-bridge diode rectifier. This topology is suitable for battery charging application with reduced losses and better power quality.

Keywords: *AC-DC Converter, half-bridge, single-stage, power factor correction*

1.0. INTRODUCTION

The advancement in power electronics technology have enabled the development of single stage AC-DC converters. Dual stage AC-DC converters introduce more harmonics and switching losses which affects the efficiency of the system. So recent researches are emphasizing more on reducing the number of power electronic components along with increasing the efficiency. The power electronic equipments cause harmonics which results in poor power factor, lower efficiency and higher cost. So Power-Factor-Correction (PFC) technique has been widely used in AC-DC power electronics systems [1-10]. Active PFC technique consists of two-stage and single-stage approaches. The two-stage PFC consists of two power conversion stages, which is commonly used. The front-stage is a PFC circuit followed by a DC-DC converter which gives a higher power factor, low voltage stress and output voltage regulation. High cost and lower efficiency due to two stage power processing are some of the demerits [3].

In the recent years, to solve the above described problems, single stage power factor corrected AC to DC converters are used. The two power stages of the PFC circuit and DC-DC converter are simplified by sharing a common switch or a pair of switches [4]. The single stage power factor correction scheme sharing only one active switch for the PFC stage and DC-DC converter has been implemented [5]. The structure of these converters is simple. They are widely used in industrial applications like ballast and battery chargers. The PFC and DC-DC regulation are carried out in cascade two stages. These converters have larger switching losses as a result of hard switching. Therefore, the efficiency of this type of single stage PFC is low.

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Flyback and forward converters are commonly used topologies for PFC. In a conventional flyback converter, hard switching of power switches causes high switching losses and high switch voltage stress. To compensate this, asymmetrical half-bridge DC-DC converters has been developed. [6-7]. The single-stage PFC AC-DC converters use full-bridge diode rectifier which increases the conduction losses and decreases the power efficiency. At low line voltages, the full-bridge diode rectifier causes high conduction losses. These problems can be overcome by eliminating the full-bridge diode rectifier. This paper proposes a single-stage half-bridge AC-DC converter which integrates the bridgeless boost rectifier [10-12] with the Asymmetrical Pulse-Width Modulation (APWM) half-bridge DC-DC converter [13-15].

This converter provides an isolated DC output voltage without using any full-bridge diode rectifier. Conduction losses are lowered by eliminating the full-bridge diode rectifier. This converter gives a high power factor and low cost. Thus it can reduce the power factor penalties imposed on industrial users and thus reduce the cost of electricity bills. The experimental hardware prototype is designed to get a regulated output of 15 V which can be used for low power applications, specially as battery chargers. The converter topology and operation are explained in section 2 and 3 along with simulation results. Section 4 gives the hardware implementation of the proposed topology with results obtained.

2.0. CONVERTER TOPOLOGY

The APWM half-bridge DC-DC converter consists of the dc-link capacitor C, blocking capacitor C_3, transformer Ti, output diode D_3 and output capacitor Co. Figure 1 shows the circuit diagram of the single-stage half-bridge AC-DC converter. In this converter, the PFC circuit and the APWM half-bridge DC-DC converter are integrated and thus the full- bridge diode rectifier is not needed. C_1 and C_2 are output capacitors of MOSFETs S_1 and S_2 respectively. D_1 and D_2 are body diodes of S_1 and S_2 respectively. The circuit topology is shown in Figure 1, which is in mode1 operation.

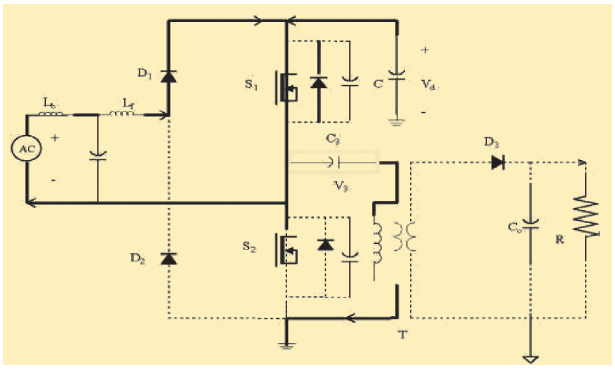

FIG. 1 CIRCUIT TOPOLOGY (MODE 1)

The line voltage, V is given by

$$G_c(s) = \mathrm{Kp}(1 + \frac{1}{\mathrm{T_i}s}) \quad \text{....(1)}$$

where V_{in} is the Root-Mean-Square (rms) value and ω is the angular frequency of Vi. ωt = 2πf line where f_{line} is the line frequency. For a positive half cycle of the input voltage, the ac line voltage is connected to the terminal of the dc-link voltage V_c through D_i. For the negative half cycle of the input voltage, the ac line voltage is connected to the ground through D_2. R is the load resistor and is is the instantaneous load current. The capacitors C, C_3 and Co are large enough so that the voltages V, V_3 and V_o are constant. The transformer has a magnetizing inductor Lm and turns ratio of 1 : N. Si is controlled with the duty ratio D. S and S_2 have conduction times of DTs and (1-D) T_S respectively. When Si is turned ON, the input current flows through L_b, Di and Si. When Si is turned OFF, the input current flows through L_b, D_i, C_d, S_2 and DS_2.

2.1. Controller Model

The control circuit for power factor correction and output voltage regulation which consists of two PI type compensators with the transfer function

$$V = \sqrt{2}V_{in}\mathrm{Sin}\,(\omega t) \quad \text{....(2)}$$

where Kp and T_i are the proportional gain and integral time constant respectively. The control scheme is shown in Figure 2. The output voltage

is regulated by the outer PI controller and power factor correction is done by the inner PI controller. The outer PI controller maintains constant output voltage even if the load or the input voltage changes. The inner PI controller optimizes PWM pulses so that input current and input voltage are in phase and distortion is less.

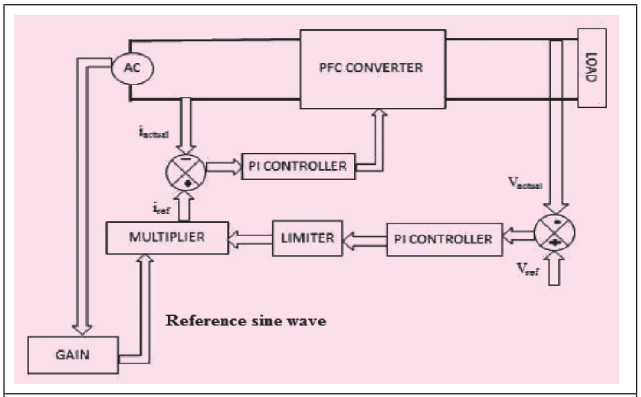

FIG. 2 CONTROLLER MODEL

3.0. CONVERTER OPERATION

There are fives modes of operation for the single-stage half-bridge AC-DC converter. Figure 2 shows the operation modes of the converter [2]. Figure 3 shows the operation waveforms of the converter.

3.1. Modes of Operation

Mode 1 [t_0, t_1] : Gating signal is applied to the gate of S_1 at t = to. The boost inductor L_b stores energy from the input AC line voltage.

Mode 2 [t_1, t_2] : S_1 is turned off at t = t_1. The magnetizing inductor current and boost inductor current are constant. The primary current charges C_{S1} and discharges C_{S2}. Operation shown in Figure 3.

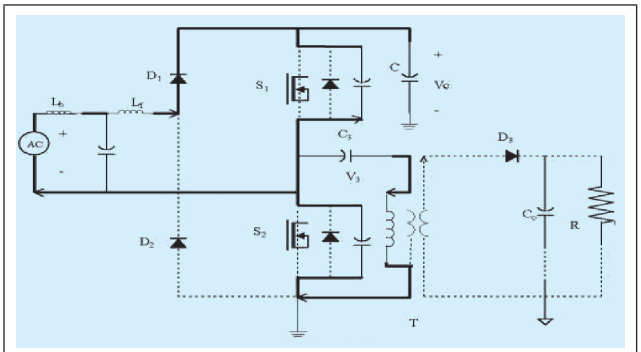

FIG. 3 CONVERTER OPERATION- MODE 2

Mode 3 [t_2, t_3] : Gating signal is applied to S_2 at t = t_2. The boost inductor current decreases. The energy stored in the boost inductor is released to the dc-link capacitor. The output diode D_o is turned ON. Operation shown in Figure 4.

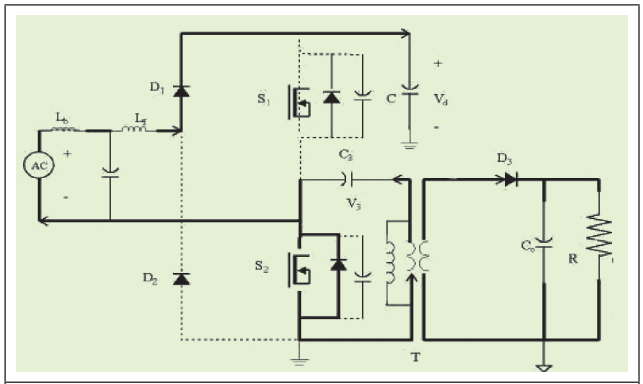

FIG. 4 CONVERTER OPERATION- MODE 3

Mode 4 [t_3, t_4] : The boost inductor current is zero at t=t_3. D_3 is turned off. The magnetizing inductor current and primary current are equal.

Mode 5 [t_4, t_5] : S_2 is turned off at t = t_4. The primary current charges C_{S2} and discharges C_{S1}. The voltage across switch S_1 is zero at t=t_5. The wave forms with respect to the various modes of operation is shown in Figure 5.

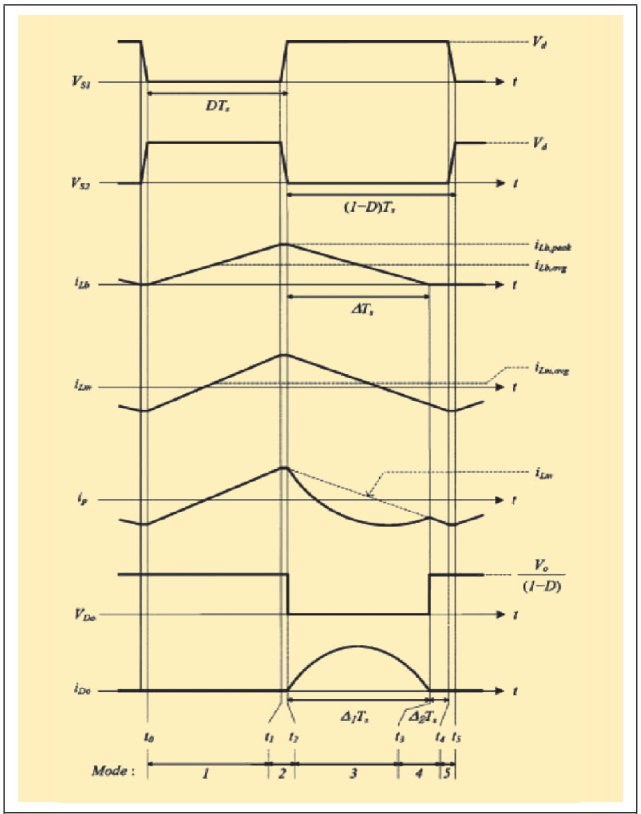

FIG. 5 CONVERTER OPERATION WAVEFORMS

3.2. Simulation Results

The following parameters are used for simulation of the converter in PSIM™ simulation software (Table 1) :

TABLE 1			
PARAMETER VALUES			
Sl. No	**Parameter**	**Value**	**Unit**
1	Line voltage V_{rms}	90-230	V
2	Output Voltage V_o	200	V
3	Output power P_o	180	W
4	Load current Io	0.9	A
5	Boost inductor L_b	30	pH
6	Magnetizing inductor L_m	130	pH
7	Turns ratio N	2.3	--
8	Dc-link capacitor C	220	pF
9	Blocking capacitor C_3	1	pF
10	Switch output capacitors C_1, C_2	500	pF
11	Output capacitor C_o	2200	pF
12	Switching frequency f_s	50	kHz

Table 2 gives the output voltage and power factor for various rms values of input voltages. The power factor slightly reduces as the line voltage increases and fairly high for low voltage.

TABLE 2		
EXPERIMENTAL VALUES		
RMS value of input voltage	**Output voltage voltage**	**Power factor**
190	200	0.97
230	200	0.96
265	205	0.94

Figure 6 shows the boost inductor current i_{Lb} and switch gating signals V_{gs1} and V_{gs2} for an output power of 180 W. The gating signals V_{gs1} and V_{gs2} are complementary each other.

Figure 12. Input voltage, input current and output voltage at 230 V rms input voltage.

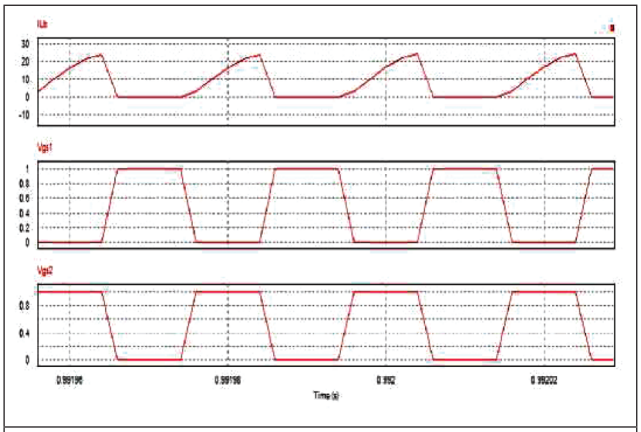

FIG. 6 BOOST INDUCTOR CURRENT I_{LB}AND SWITCH GATING SIGNALS V_{GS1} AND VGS2.

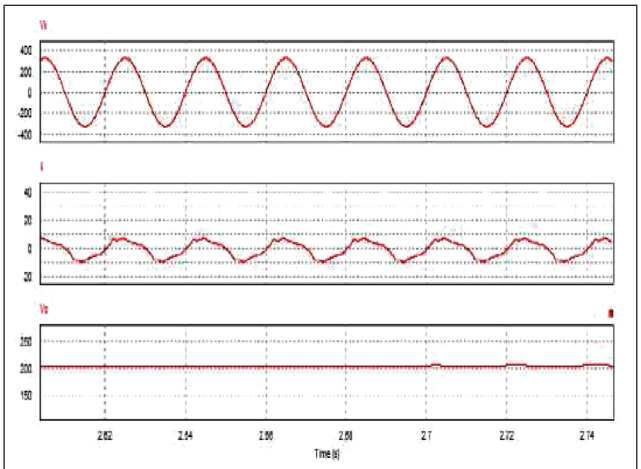

FIG. 7 INPUT VOLTAGE, INPUT CURRENT AND OUTPUT VOLTAGE AT 230 V RMS INPUT VOLTAGE.

4.0 HARDWARE IMPLEMENTATION

The hardware model of AC-DC converter using asymmetrical half-bridge flyback is tested for an input rms voltage of 120 V to get a regulated output voltage of 15 V. The switching frequency is 50 kHz. AVR microcontroller is the main control device used.

The inductors selected are

1. Filter inductor L_f as 30 mH.
2. Boost inductor L_b as 2 mH.

The core selected for the filter inductor and boost inductor are E55 and E42 respectively.

The area product equation for the inductor is given by

$$A_P = \frac{LI_p I_{rms}}{K_w B_m J} \quad \text{....(3)}$$

where L is the inductance value, I_p is the peak inductor current value, I_{rms} is the rms value of current

K_w = winding factor

B_m = maximum flux density in Weber/m2

J = current density in amperes

K_w varies from 0.2 to 0.35, J ranges from 2 to 5A/mm2 and B_m ranges from 0.2 to 0.35.'

For filter inductor

$$A_p = \frac{30\times10^{-3}\times3\times1.86}{0.35\times3\times0.3\times10^{-6}} = 53.14\times10^4 mm^2 \quad \text{....(4)}$$

E42 core is selected for this inductor.

For boost inductor

$$A_p = \frac{30\times10^{-6}\times13.65\times50}{0.35\times3\times0.3\times10^{-6}} = 6.5\times10^4 mm^2 \quad \text{....(5)}$$

E42 core is selected for this inductor.

The capacitor values selected are dc-link capacitor as 220 µF, blocking capacitor as 1 µF, output capacitor as 2200 µF, filter capacitor as 1.25 µF. All the capacitors are of electrolytic type. They are selected based on the voltage ratings.

Mosfet used is IRF 840 having a Drain to Source voltage VDS of 500 V. Diodes used are MUR1560. They are ultrafast recovery diodes having a voltage capability of 600.

An asymmetrical half-bridge flyback converter is used that has a turns ratio of 2.75. The maximum duty cycle is 0.5. The number of primary turns is 25 and the number of secondary turns is 9. E42 core is selected for the transformer.

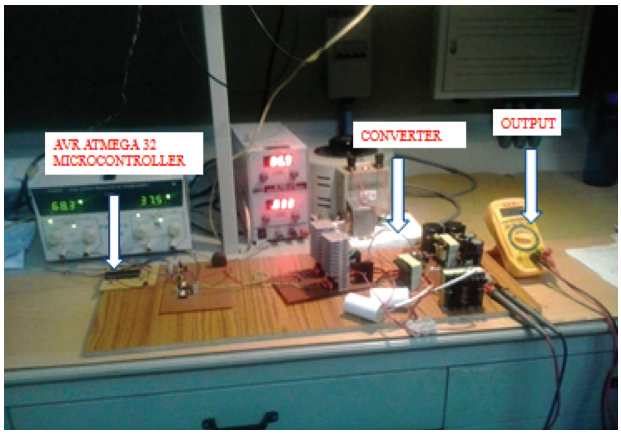

FIG. 8 EXPERIMENTAL SET UP

Figure 8 shows the experimental setup that consists of supply part, linear voltage regulator circuit, gate driver circuit, converter circuit, AVR ATMEGA 32 microcontroller and load side.

The switching pulse to drive the switch S_1 and voltage across the switch S_1 are shown in the Figure 9. Figure 15 represents the switching pulse to drive the switch S_2 and voltage across the switch S_2. These waveforms are an indication of Zero Voltage Switching of the switches. Figure 10 shows the output voltage waveform of the converter. The maximum output voltage obtained is 15.2 V. Figure 11 gives the power analyzer waveforms of the input voltage and input current. Figure 13 shows the power analyzer displaying input power factor 0.97.

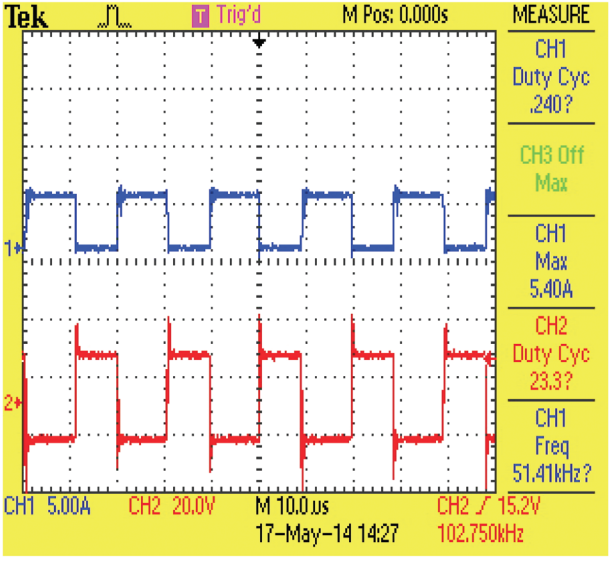

FIG. 9 SWITCHING PULSE AND VOLTAGE ACROSS SWITCH S_1

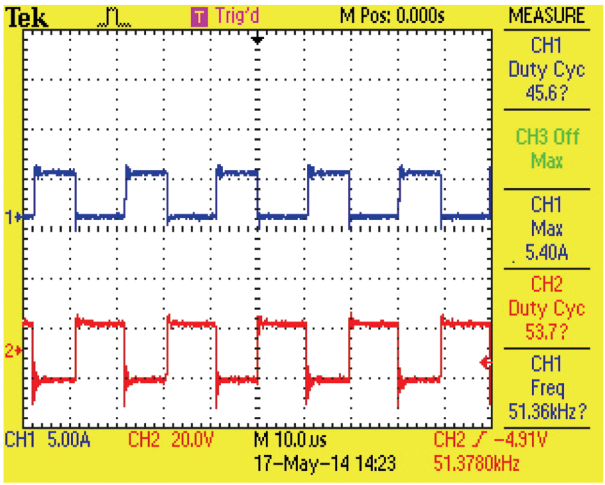

FIG. 10 SWITCHING PULSE AND VOLTAGE ACROSS SWITCH S_2

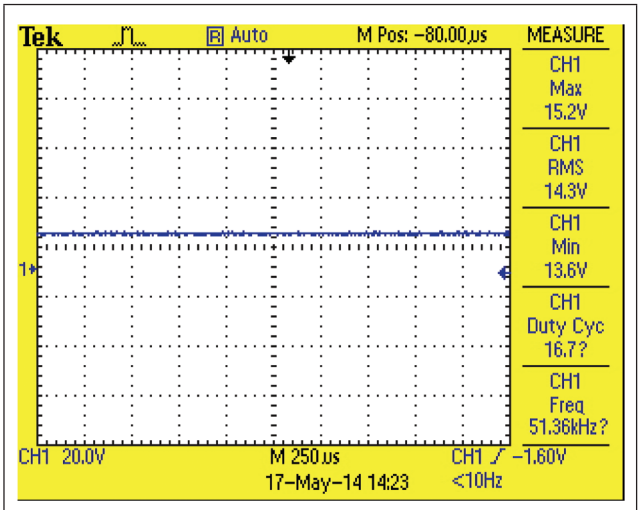

FIG. 11 OUTPUT VOLTAGE WAVEFORM

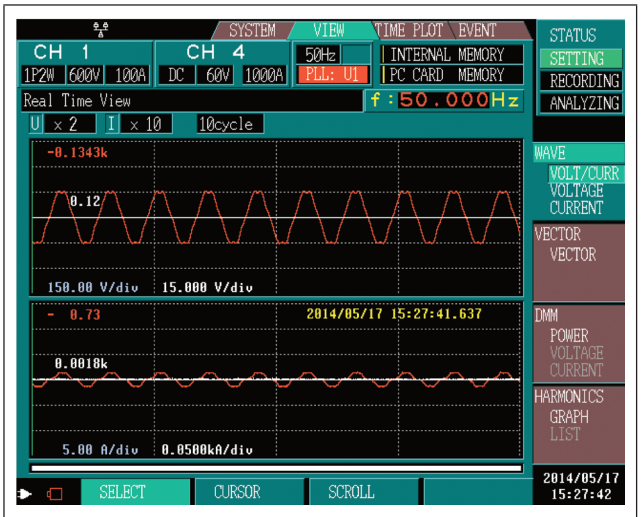

FIG. 12 POWER ANALYZER WAVEFORMS OF INPUT VOLTAGE AND INPUT CURRENT

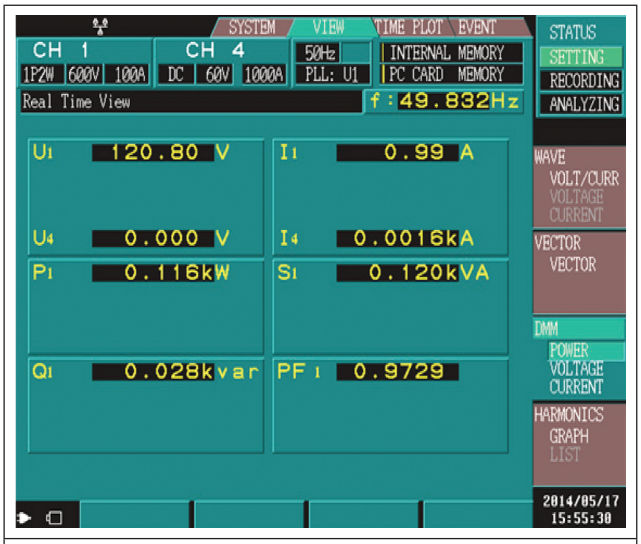

FIG. 13 POWER ANALYZER DISPLAYING POWER FACTOR

5.0. CONCLUSIONS

The converter provides an isolated DC output voltage without using any full-bridge diode rectifier. Conduction losses are lowered by eliminating the full-bridge diode rectifier. This converter have high power factor and low cost. The closed loop simulation shows that the output voltage is regulated to 200 V with variation in input voltage and improvement in power factor. The experimental results also validate the same.

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