



Application of Superconducting Fault Current Limiter and Chopper Controlled Resistor for Protection of VSC-HVDC Systems

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Abstract

The Voltage Source Converter based HVDC (VSC-HVDC) transmission system involving overhead lines lack the inherent ability to overcome severe over currents and over voltages during dc line fault conditions. Presently, the fast acting commercial HVDC circuit breakers are uneconomical and are in prototype status. Due to this, the VSC-HVDC system finds applications in back to back and underground cable transmissions where the occurrence of dc faults is almost zero. In this context, the present paper analyses the combined application of Superconducting Fault Current Limiter (SCFCL) along with Chopper Controlled Resistors (CCR) to overcome and recover from the effects of dc line faults. The resistive SCFCL is modeled in MATLAB and the VSC-HVDC system is analyzed using PSCAD/EMTDC environment. The simulation results show that during dc line faults, the SCFCL is effective in limiting the over currents and the CCR overcomes the over voltages. The combined simulated protection strategy restores the complete VSC-HVDC system without restarting of the dc link

Keywords: Voltage Source Converter based HVDC (VSC-HVDC), Superconducting Fault Current Limiter (SCFCL), Chopper Controlled Resistors (CCR)

1. Introduction

The VSC-HVDC transmission systems have gained enormous importance because of their immunity to commutation failure, lower foot prints, operation without telecommunication, and ability to control active and reactive powers independently. This opens up various application areas such as integration of renewable sources, power supply to islands, remote loads, city centre in-feed, multi-terminal dc (VSC-MTDC), DC grid operation, improvement of voltage stability and power quality¹⁻⁴.

The VSC-HVDC transmission system based on overhead lines is vulnerable to dc line faults and lack the inherent ability to overcome severe over currents and over voltages. For this reason, presently the VSC-HVDC system applications are limited to back to back and/ or underground cable systems where dc line faults are almost absent. But even in VSC-HVDC transmission networks via dc cables the dc fault transients and the fault current contribution occurring, their point of location and isolation are also of more serious concern and has a major impact on the system operation^{5–7}.

The World's first VSC-HVDC power transmission in 1997⁸ was tested on overhead lines and suggested the use of over voltage limiter i.e. chopper to discharge the over voltages and the use of dc line switches for fast isolation. In a major application, the World's first commercial VSC-HVDC system based on dc overhead lines^{9.10} came into operation in 2011. Here, the difficulties of dc line fault conditions are overcome by using a combination of dc switches and ac circuit breakers. It has to be noted here

that this necessitates complete shutdown and re-starting of the VSC-HVDC transmission link. For the same reasons, the application of this method, in multi-terminal VSC-HVDC (VSC-MTDC) system with overhead lines may not be possible.

The protection of VSC based point to point and MTDC systems is of utmost concern and has attracted many researchers to come up with different possible solutions to overcome dc line fault conditions. The authors in¹¹⁻¹⁴ suggested the use of controllers, ac and dc breakers/ switches to overcome dc faults. Franck in¹⁵ presented an extensive review of the status and developments of HVDC circuit breakers. Also, identified the focusing areas of research for dc circuit breaking including fault current limiters are suggested. In order to overcome dc line fault transients the paper¹⁶ have outlined the options and methods of realizing HVDC breakers, clearing and isolating dc faults, varying ac and dc system parameters, using dc side SCFCL and placing circuit breakers at strategic grid locations. To overcome the dc faults in VSC Modular Multilevel Converter (MMC-HVDC) with overhead lines the configurations, controls, and recovery conditions are studied in¹⁷⁻¹⁸. For HVDC grid operation¹⁹ the concept of using current limiting inductors in combination with hybrid DC breakers is presented. The study in²⁰ reported the use of superconducting fault current limiter to reduce the current breaking burden of hybrid HVDC breaker in a HVDC grid.

The VSC-HVDC systems are incorporated with Surge Arrestors on each dc pole to protect from transient over voltages such as lightning and switching surges²¹. During dc line fault conditions, due to dc voltage controller even the use of Surge Arrestors will not help to limit the dc pole over voltages and during such conditions the possible solutions of system recovery are studied in^{22–24}. To isolate the HVDC grid from dc faults²⁵ suggested the application of semiconductor based protection devices like series hybrid dc breaker, half bridge and full bridge dc choppers, and LCL thyristor converter configurations. Here the Surge Arrestors are used to limit the over voltages and absorb the fault energy after breaker isolation. The over voltages are caused in Wind farms connected VSC-HVDC system due to ac faults on onshore ac grid. The paper²⁶ proposed the application of Chopper Controlled Resistors (CCR) to overcome such over voltages.

From the above discussion, it is observed here that the controllers along with some type of dc protective devices are best suited to obtain a satisfactory recovery and transient performance, and also to isolate the dc line during a permanent fault. Also, very limited results are available to show the application of CCR in VSC-HVDC system to overcome the dc line fault condition.

The present day challenge is to quickly overcome the severe over currents and over voltages caused during dc faults and to recover the system without necessitating the complete shutdown which causes long duration transmission interruption. The application of fast acting HVDC circuit breakers can quickly extinguish the dc fault current and isolate the dc link. But, the fast acting commercial HVDC circuit breakers are uneconomical and still in prototype status²⁷. Hence, there is a strong need to study and design alternative HVDC circuit breaking protection schemes with available technologies and to extend these protection concepts to VSC-HVDC grid networks.

In this context, a Superconducting Fault Current Limiter (SCFCL) with ultra-fast switching capability can be an attractive alternative. The present author's in²⁸carried out a detailed study of resistive SCFCL covering material aspects, dynamic modelling and its application in low voltage VSC-HVDC system to mitigate the effects of DC line fault conditions. The focus of the study was to overcome and limit the large dc currents during dc line faults. The results of these studies indicate the usefulness of SCFCL in controlling the over currents during transients. However, the problem of over voltages during the dc line fault was not addressed. These difficulties and the methods to overcome the effects of dc line fault were addressed in a continued work²⁹. However, imbalance of voltages existed in the system due to severe ac line faults and the complete recovery of voltages was not addressed. The application of SCFCL in upcoming multi-terminal UHVDC system in India³⁰ indicated the effectiveness and ability to clip the fault currents to lower values within a half a cycle in MTDC system.

The present paper has combined the applications of resistive SCFCL and CCR devices in a VSC-HVDC system involving dc overhead lines to control over currents and over voltages during dc line fault conditions. The simulation results using PSCAD/EMTDC environment in case of dc line faults indicate that the SCFCL efficiently limits the fault currents during both ac and dc faults to low values and the CCR device controls the over voltages on healthy pole in a remarkable manner. The behaviour and operation of VSC-HVDC system is affected when these devices considered separately and combined. The result



Figure 1. Schematic of two terminal VSC-HVDC system.

shown helps in contingency conditions when any one device goes out of service.

2. Protection of VSC-HVDC System

A schematic of VSC-HVDC system with overhead transmission lines is shown in Figure 1. In the present study the superconducting fault current limiter and chopper controlled resistors are applied to overcome the dc line fault conditions. The work carried out by present author's in^{28–30} explains the basics of SCFCL and CCR. The operation of VSC converter during dc fault, the details of SCFCL and CCR used in the present study are presented here for completeness.

2.1 DC Line Fault Condition

Figure 2 shows the converter of VSC-HVDC system with overhead lines under dc line to ground fault condition. During the dc side fault, it is observed here that even if blocked, the IGBTs lose control and the freewheeling anti-parallel diodes act as uncontrolled bridge rectifier and feed the fault resulting in large dc line current [24]. As a result of this the dc capacitor on the faulted line starts discharging into the fault and because of the dc voltage controller the voltage of the healthy pole increases to a very high value about 2 pu and the voltage of faulted pole goes to almost zero. This creates unbalanced conditions and imbalance of dc pole voltages. The protection strategy has to be such that it limits the over currents and rebalances the dc pole voltages without necessitating blocking of the VSC converters.

2.2 Superconducting Fault Current Limiter

A Fault Current Limiter (FCL) fundamentally offers a very high impedance to fault current bringing it down to a low value in a very short time. SCFCL is one of the technically and economically attractive alternatives to limit the peak value of fault current quickly (within half cycle). The SCFCL will be in superconducting state offering zero resistance during normal operation and transits to normal resistive state and offers high impedance during fault conditions. They have distinct advantages over conventional FCLs in high voltage networks. SCFCL provides an ultrafast transition from superconducting to normal state and is self-operating and repetitive in nature. Further, during normal operation the resistance being zero and the losses will be negligibly small.

At present, the SCFCL applications are mostly concentrated in ac systems. Various prototype ac SCFCLs have been designed and successfully field tested, demonstrating their technical feasibility. A number of High Temperature Superconducting (HTS) materials working at 77 K have been suggested for power system applications. Of these, Bi2212 is one of the most robust material and artifacts with large surface area can be produced. This means that for the same critical current the critical current density of the FCL can be made higher and hence Bi2212 based FCLs can have higher ratings.

Among the various SCFCLs the resistive SCFCL has been proposed for power system applications. This is because the operation of the resistive type SCFCL is simple to understand, can be easily connected in series-



Figure 2. VSC converter- dc capacitors and freewheeling diodes feeding the dc fault.

parallel combinations, reduces the time constant of the aperiodic component of the fault current and can also make the system less inductive. A number of studies concerning material aspects, types of SCFCLs, prototypes and testing have been carried out in detail in^{31–35}. Further, various researchers in this field, have come up with the concepts, studies and field testing of SCFCL devices for transmission level voltages. The matrix SCFCL module is obtained by connecting the basic SCFCL elements in series and parallel. A detailed study of this along with field test results is outlined in^{36–39}.

The application of SCFCL in HVDC systems has received limited attention but is gaining importance. Some of the conceptual details, materials and test results of DC-SCFCL are explained in detailed in^{40–42}. In 2014 the researchers' in⁴³ designed and constructed a prototype matrix type DC resistive SCFCL for real HVDC application. The critical current capability of SCFCL module is 5 kA. The matrix SCFCL consists of basic ten (10) SCFCL units each with critical current capability of 500 A. The experimental and test results demonstrated the current limiting capability of SCFCL in dc system including the different values of shunt resistor to limit the heat and temperature across SCFCL.

2.3 Mathematical Model of SCFCL

The E-J characteristic⁴⁴ exhibited by all HTS materials is shown in Figure 3. The behaviour of the HTS-SCFCL device is governed by this nonlinear E-J characteristic which exhibits very strong dependence on temperature. When the current density in the SCFCL exceeds the critical value, an electric field develops across the FCL. The electric field thus developed at any instant depends upon



Figure 3. E-J characteristic of HTS material.

the current density in the SCFCL and the temperature of the FCL. This E-J characteristic forms the basis for the modelling and simulation of SCFCL. The E-J characteristic can be subdivided in to 3 parts:

2.3.1 Superconducting State

In this state, the HTS material is in the superconducting state. The current density across SCFCL is below the critical value and consequently the electric field across it is very small. The electric field is given by

$$E(J,T) = E_c \left[\frac{J}{J_c(T)}\right]^{\alpha}$$
(1)

Here $J_c(T)$ is the critical current density, T is temperature of the superconductor, E_c corresponding electric field, and J is current density of Bi2212 material. The quantity $J_c(T)$ is temperature dependent and this dependence obtained experimentally is taken to be,

$$J_{c}(T) = \frac{J_{c}(77)(T_{c} - T)}{(T_{c} - 77)^{1.8}}$$
(2)

with temperatures expressed in the units of K. Here Tc is the critical temperature of the superconductor.

2.3.2 Flux Flow State

The HTS material enters this state when the current density across it exceeds a value represented by J0. In this state, because of higher value of the current density, the electric field across the FCL starts picking up and the FCL develops resistance. Because of this resistance, the temperature increases. This increase in temperature causes a further increase in electric field across the FCL. This is self-enhancing process and it continues until the temperature of FCL exceeds a critical value known as critical temperature. At this point, the HTS material enters the normal resistive state. During this phase the electric field is given by,

$$E(J,T) = E_0 \left(\frac{E_c}{E_0}\right)^{\left(\frac{\beta}{\alpha}\right)} \frac{J_c(77)}{J_c(T)} \left(\frac{J}{J_c(77)}\right)^{\beta}$$
(3)

2.3.3 Normal Resistive State

In this state the normal conducting properties of the HTS material are exhibited. Here, the electric field across FCL is linearly proportional to both current density and the temperature of the FCL and is given by,

$$E(J,T) = \rho(T_c) \frac{T}{T_c} J$$
(4)

Here, ρ is the normal resistivity. For bulk Bi2212 material, the parameters $J_c(77), \rho, \alpha, \beta$ at 77 K depend upon the material processing condition and falls in the following range: $10^7 " J_c" 10^8$ A/m2, $0.1 " E_0" 10$ mV/cm, $100 \le \rho \le 200 \mu \Omega$ -cm, $5 \le \alpha \le 15$, and $2 \le \beta \le 4$.

These parameters have to be chosen carefully because they bring about a marked difference in the behaviour of FCL. In all the three states mentioned above, the heat diffusion equation of the HTS material is given by,

$$c\frac{dT}{dt} = E(J,T)J \tag{5}$$

where, c = specific heat of Bi2212 which is again temperature dependent.

Modelling the behaviour of SCFCL involves the following steps. Knowing the cross sectional area and current flowing through the superconductor, calculate the current density in the SCFCL at each instant and compare the electric field E(J,T) with E0. With E(J,T) \leq E0, FCL is in the superconducting state. When E(J,T) > E0, SCFCL enters the flux flow state. SCFCL continues to be in flux flow state till R_{FCL} " R_n , where $R_n = \rho(90)Ln/S$ and Ln and S are length and area of cross section of the superconducting material. When R_{FCL} " R_n , the FCL is in normal state and offers maximum resistance to the flow of current. The electric field, voltage drop, temperature and resistance of the SCFCL are calculated at every instant.

For the present study, the SCFCL model described above using E-J characteristic is modelled in MATLAB and the simulation results are presented in previous paper²⁸ by the present authors. This model is tested and validated according to the method suggested, data and results available in^{44.45}.



Figure 4. Chopper controlled resistor.

2.4 Chopper Controlled Resistor

The schematic of CCR is shown in Figure 4. The CCR consists of an IGBT switch T with anti-parallel diode D and a series resistor Rc. In the present study, the CCRs are used across the dc capacitors of VSC converter. The aim here is to suppress the over voltages during dc faults and make the recovery of the VSC-HVDC system smooth.

The operation of CCR is as follows. During dc line fault, when the voltage across the dc capacitors increase to high value the IGBT switch T is turned ON through a triggering pulse Tc and the dc capacitor voltage is discharged through resistor Rc. When the dc voltage reaches an acceptable value the switch T is turned OFF. Thus, by using CCR across each dc pole capacitor, the dc line voltages can be brought to normal values in a controlled manner. The value of resistor Rc decides the discharging current and the rate at which the voltage is discharged.

3. Selection of System Parameters

For the present study, this section discusses the selection of different parameters for VSC-HVDC system, SCFCL and CCR devices.

3.1 VSC-HVDC Parameters

A schematic of VSC-HVDC system with overhead transmission lines is shown in Figure 1. For the present study, the system with ratings \pm 110 kV, 2.8 kA, 600 MW is developed, modelled and the results of dynamic analysis for ac and dc fault conditions are presented using PSCAD/ EMTDC environment. Table 1 gives system parameters. The focus of the study is to overcome DC fault conditions using SCFCL and CCR devices. The AC system impedance is considered as The venin's equivalent circuit. The two converters VSC1 and VSC2 are of 2 level, 6 pulse, symmetrical monopole, and point to point configuration with centre point of the dc capacitors across each converter grounded. Each VSC can transmit power in either direction, but in this study the power transmission is from VSC1 to VSC2.

Generally, the rating of each VSC-HVDC converter is twice the rated value of the transmission system. Any value above the maximum rating the VSC's have to be tripped otherwise it will break. In this study the parameters of the system are considered such that the maximum total fault current with protective devices in the dc line not to exceed 2 times the rated value 2.8 kA. This is done by considering values of transformer reactance, converter phase reactor is taken for the purpose of electrical measurements also helps to reduce rate of rise of fault current and a series dc reactor at each VSC to reduce the ripple, dc fault current derivatives and control charge across dc capacitor. The dc line model is considered as equivalent T model. The dc link capacitor at each VSC helps to maintain the steady dc bus voltage and avoids voltage collapse. Here, the value is considered based on the method suggested and data given in⁴⁶.

Parameter	Value				
VSC-HVDC:					
Total Rated Power	600 MW				
DC Voltage	± 110 kV				
DC Current	2.8 kA				
Converter Phase Reactor (L_p)	0.004 H				
AC filter capacitor (C_f)	18 µF				
DC link capacitor (C)	500 μF				
DC reactor (L _{dc})	0.002 H				
Switching frequency (p)	27 times				
AC System	VSC1	VSC2			
AC Voltage (L-L, RMS)	330 kV	230 kV			
Frequency	50 Hz	50 Hz			
Impedance (Z_{Th})	9.075 Ohm	5.8 Ohm			
Impedance Angle	80 deg.	80 deg.			
X/R ratio	5.7	5.7			
Transformer ratings	550 MVA, 330/ 115 kV, X _t = 0.06 pu	550 MVA, 230/ 115 kV, X _t = 0.06 pu			
DC Line (equivalent T model)					
Length	50 km				
Resistance R _{dc}	1.76 Ohm				
Capacitance $C_{dc(Line)}$	24 µF				

	Table	1.	VSC-	HVI	DC s	ystem	parameters
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The converter controllers dramatically influence the dynamic behaviour of the dc link. The different controllers used with each converter of VSC-HVDC are outlined in⁴⁷. The controllers are decided based on the function of the VSC-HVDC system. Here in the present study the dc link is transmitting 600 MW of power to inverter (VSC2)

side ac system. After obtaining satisfactory steady state and transient behaviour with different combination of controllers, the controllers used here are dc voltage and ac voltage controls for VSC1 and active power and ac voltage controls for VSC2.

3.2 SCFCL and CCR Parameters

The SCFCL model is developed in MATLAB and interfaced with the VSC-HVDC system in PSCAD/EMTDC environment and the various transient conditions are studied to understand the effectiveness of the SCFCL on the performance of the system. In the present work, the required rating of SCFCL module is 110 kV, 2.8 kA, 300 MW and for this rating a matrix SCFCL module is used. A number of lower rated SCFCLs are connected in series-parallel to make up the required rating. Each individual SCFCL component is rated for 10.5 kV and 2.0 kA (both rms). Ten such components in series result in 110 kV and 2.8 kA (peak). This SCFCL model is tested and validated. The parameters of SCFCL used for the present work are given in Table 2.

For CCR device, the value of resistor Rc is chosen as Rchopper = 240 Ohm, and CCR is triggered when the threshold value of dc pole voltage reaches 30 % more (1.3 pu).

Table 2. SCFCL parameters

Parameter	Value
Rated voltage U _N	10.5 kV
Rated current $I_{_{\rm N}}$	2 kA, 2.8 kA (peak)
MVA S _N	21
Initial operating temperature (T)	77 K
Critical operating temperature (T_c)	90 K
Critical current density at 77 K (J_c 77)	1.5e7 A/m ²
Electric field at transition from Superconducting to Flux-flow state (E_0)	1 V/m
Critical Electric field (E_c)	1.0e-4 V/m
Length of superconductor (l_{sc})	20 m
Superconducting region exponent at 77 K (α)	4
Flux-flow region exponent (β)	2.5
Cross section of Superconductor (S)	0.34e-4 m ²
Normal conducting state resistivity (ρ)	7e-6 Ω-m
Self inductance (L_{sc})	0.4e-6 H
Shunt resistance (R _{sh})	2 Ω



Figure 5. VSC-HVDC system with SCFCL and CCR devices.

4. Analysis of VSC-HVDC System

This section analyses the performance and usefulness of SCFCL and CCR devices integrated with VSC-HVDC system involving dc overhead lines in PSCAD/EMTDC environment. The SCFCL can be placed in series with dc line, either on the rectifier side or on the inverter side. Figure 5 shows the schematic diagram of a 110 kV, 2.8 kA, 600 MW, VSC-HVDC system, with SCFCL and CCR devices. The SCFCL is connected on the inverter side in series with the dc line.

The aim of this study is to investigate and evaluate the performance of the VSC-HVDC system with SCFCL and CCR devices for various dynamic ac and dc fault conditions. Of specific interest is the dc line fault. The time step chosen for the simulations is $\Delta t = 50 \ \mu S$. This is sufficient to notice the behavior of SCFCL which provides ultra-fast transition from superconducting state to normal state. After establishing satisfactory steady state behavior different transient conditions such as three phase to ground fault on inverter ac bus and dc line to ground fault at dc side of VSC2 are created to study and assess the behavior of SCFCL and CCR devices for smooth recovery of the system In all the cases presented here, the faults are created at 1.2 sec lasting for duration of 3 cycles.

The behavior and operation of VSC-HVDC system affected has been discussed when SCFCL and CCR devices considered separately and combined which will help in contingency conditions when any one device goes out of service.

In the present study, the protection using mainly SCFCL and CCR are considered without including impact of HVDC breakers. The aim is to reduce over voltages and over currents without considering the operation of the HVDC breakers. The operation including circuit breakers will be dealt in a separate publication.

5. Results and Discussions

5.1 Three Phase AC bus Fault

In order to investigate the behaviour of resistive SCFCL and CCR devices in VSC-HVDC system, a three phase to ground fault at inverter ac bus is created at 1.2 sec lasting for duration of 3 cycles. The variation of dc voltages and dc currents measured at dc side of VSC1 converter are compared for the cases with and without SCFCL and CCR devices along with the behaviour of the devices. These plots are shown in Figure 6(a) to 6(f) and Figure 7.

5.1.1 Without SCFCL and Without CCR

During the fault period without SCFCL and without CCR the dc voltage of positive pole reached the maximum value of about 165 kV from steady state value of 110 kV and this value for negative pole is about -170 kV, as in Figure 6 (a) and (b). For the same case, the dc current at the positive pole increased rapidly and reached the maximum values of 5 kA, -2.8 kA and then reached up to 10 kA, from a steady state value of 2.8 kA. This also resulted in the variation of dc current of the negative pole. The peak current reached a value of -5 kA, 2.8 kA and then -10 kA.

5.1.2 With SCFCL and Without CCR

For the case with SCFCL and without CCR, with the increase in the current, the temperature of SCFCL increases and it loses superconductivity and transits to normal state. This introduces a resistance in the circuit which clips the first peak of the fault current. The peak value of line current, at positive pole, is reduced from 5 kA to 4 kA. Subsequent peaks are also clipped as in Fig. 6(d). A similar variation can be seen for the negative pole current and is indicated in Fig. 6(e). The dc voltages of



Figure 6. System performance for three phases to ground fault with and without SCFCL and CCR devices. (a) DC voltage at positive pole. (b) DC voltage at negative pole. (c) DC voltages across CCR. (d) DC current at positive pole. (e) DC current at negative pole. (f) Discharge Currents of CCR.

both the poles reached the magnitudes of 140 kV (positive pole) instead of 165 kV and -160 kV (negative pole) instead of -170 kV respectively. While the currents at both poles reached the steady state value, the voltage of positive pole stays at 120 kV instead of 110 kV and negative pole voltage remained at -100 kV.

5.1.3 Without SCFCL and With CCR

In this case without SCFCL and with CCR, when the voltage across each pole increased to about 30 % (cho-

sen value in the present case), the CCR device is triggered ON through a pulse. This resulted in discharging of over voltage across each pole to ground through a resistor Rc. Gradually the over voltages across each pole decreases and within a short duration, the system is recovered reaching the rated steady state values of voltages. At this point, the CCR is triggered OFF. The voltages across CCR and discharge currents are shown in Figure 6(c) and 6(f). Thus, use of chopper controlled resistor resulted in control of over voltages quickly in few milliseconds. The dc



Figure 7. Behaviour of SCFCL for three phase fault.

voltages of both the poles reached the magnitudes of 140 kV (positive pole) instead of 165 kV and -160 kV (negative pole) instead of -170 kV respectively. This in turn helps in reducing the current peaks at both positive and negative poles as indicated by the plots. The positive pole current reached a maximum of 5.6 kA instead of 10 kA and the same for negative pole reached -5.6 kA instead of -10 kA. Thus CCR device controls over voltages and also limits over currents.

5.1.4 With SCFCL and With CCR

For the case with both SCFCL and CCR devices in the system, the SCFCL within half a cycle reduces the first peak value of dc currents of positive and negative poles to 4 kA and -5 kA respectively. The dc voltages of both the poles reached the magnitudes of 140 kV (positive pole) and -150 kV (negative pole) instead of experiencing over voltages.

Thus, when both SCFCL and CCR devices included in the circuit, the dc currents and dc voltages reached steady state values within the first few milliseconds in a short duration and system recovered smoothly without shutdown of the system.

The behaviour of SCFCL device i.e. the temperature and resistance curves are shown in Figure 7. During the fault, the SCFCL enters the normal state and HTS material develops heat across it and this must cool down, in order to regain superconductivity.

The time taken by SCFCL device to return it to superconducting state is known as recovery period and it varies from few milliseconds to seconds. The recovery characteristics of SCFCL are not considered here and will be discussed in a future study.

5.2 DC Line Fault

5.2.1 Control of DC Over Voltages using CCR

To study the behaviour of Chopper Controlled Resistor (CCR) a dc line to ground fault is created at dc side of VSC2 at 1.2 sec lasting for 3 cycles. The variation of dc voltages and dc currents measured at dc side of VSC1 converter, CCR voltage and current are studied during recovery. Figure 8, shows the comparison of different dc voltages and currents for the cases without and with CCR device during dc fault condition.

Without CCR in the circuit, the dc voltage of positive pole immediately decreased to almost zero volts from a steady state value of 110 kV, whereas the dc voltage of unfaulted negative pole as explained earlier reached twice the rated pole voltage -220 kV from a steady state value of -110 kV. For the same case, the dc current of the faulted positive pole is increased sharply; reaching the positive peak of about 8.4 kA, and this value for negative unfaulted pole is about -6.2 kA. Thus, even after the fault period, there exists imbalance of dc voltages in the system which needs rebalancing of voltages through complete shutdown of the system.

With CCR included in the system, when the voltage of the un-faulted negative pole increased to about 30% more (chosen value in the present case), the CCR device is triggered ON through a pulse. This resulted in discharging of over voltage of negative pole to ground through a resistor Rc. Gradually the over voltage of negative pole decreased and the positive pole voltage gradually started increasing from zero voltage. Within a few milliseconds of duration, the system recovered with rated steady state values for the voltages. At this point the CCR is triggered OFF. Thus, use of chopper controlled resistor resulted in control of dc over voltages and rebalancing of dc voltages without shutdown.

5.2.2 DC Line Fault Control With SCFCL and With CCR

For the dc line to ground fault created at dc side of VSC2 at 1.2 sec lasting for 3 cycles, the variation of dc voltages and dc currents measured at dc side of VSC1 converter, CCR voltage and current are shown in Figure 9 (a) to (f), for three cases, without SCFCL and without CCR, with SCFCL and without CCR, and with SCFCL and with CCR devices.



Figure 8. Performance of the system for dc line to ground fault with CCR. (a) DC voltage at positive pole. (b) DC voltage at negative pole. (c) DC voltages across CCR during recovery (d) DC current at positive pole. (e) DC current at negative pole. (f) Discharge Currents of CCR during recovery.



Figure 9. System behaviour for dc line to ground fault with SCFCL and with CCR. (a) DC voltage at positive pole. (b) DC voltage at negative pole. (c) DC voltage across CCR during recovery. (d) DC current at positive pole. (e) DC current at negative pole. (f) Discharge current of CCR during recovery.

With SCFCL and CCR devices included in the system, the SCFCL within half a cycle reduces the dc currents of positive and negative poles to 4 kA from 8.4 kA and -3 kA from -6 kA respectively. The dc voltage of positive pole reached 65 kV instead of zero volts and this value for negative un-faulted pole is -150 kV instead of -220 kV.

The impact of CCR device is as follows, when the voltage of the un-faulted negative pole increased to about 30% more (chosen value in the present case), the CCR device is triggered ON through a pulse. This resulted in discharging of over voltage (-150 kV) of negative pole to ground. Gradually, the over voltage of negative pole decreased and the positive pole voltage gradually started increasing gradually from 65 kV, both reaching steady state values. Within a few milliseconds of duration, the complete VSC-HVDC system recovered with rated steady state values for the dc voltages. At this point the CCR is triggered OFF. The voltage across CCR and discharge current of CCR during recovery are shown in Figure 9(c) and 9(f). As discussed earlier, the recovery characteristics of SCFCL are not considered here and will be discussed in a future study.

6. Conclusions

This paper has successfully integrated and evaluated the performance of 600 MW VSC-HVDC systems with resistive SCFCL and chopper controlled resistors. The results of transient analysis clearly indicate the reduction of peak value of dc fault current to lower value. The dc voltages are maintained at lower values and are balanced. The chopper controlled resistor is very efficient in limiting the over voltages rapidly within first few milliseconds. The entire system recovered quickly without re-starting of the link. Thus, commercially available SCFCL device can act as an efficient protective device to overcome the effects of dc line faults within half a cycle in VSC based HVDC systems with overhead lines. Further, studies are needed to validate and compare these simulation results with the field test results.

7. References

1. Akhmatov V, Callavik M, Franck CM, Rye SE, Ahndorf T, Bucher MK, Muller H, Schettler F, Wiget R. Technical guidelines and prestandardization work for first HVDC grids. IEEE Trans Power Delivery. 2014 Feb; 29(1):327-35. https://doi.org/10.1109/TPWRD.2013.2273978

- Bucher MK, Wiget R, Andersson G, Franck CM. Multiterminal HVDC networks- What is the preferred topology? IEEE Trans Power Delivery. 2014 Feb; 29(1):406-13. https://doi.org/10.1109/TPWRD.2013.2277552
- 3. Anderson BR. VSC transmission tutorial. CIGRE B4 Meeting, Bangalore, India; 2005 Sep.
- 4. Livermore L, Liang J, Ekanayake J. MTDC VSC technology and its applications for wind power. Proc Universities Power Engg Conference (UPEC); 2010 Sep.
- Bucher MK, Franck CM. Contribution of fault current sources in multiterminal HVDC cable networks. IEEE Trans Power Delivery. 2013 Jul; 28(3):1796-803. https://doi. org/10.1109/TPWRD.2013.2260359
- Yang J, Fletcher J, Reilly JO. Short-circuit and ground fault analyses and location in VSC based DC network cables. IEEE Trans Industrial Electronics. 2012 Oct; 59(10):3827-37. https://doi.org/10.1109/TIE.2011.2162712
- Bucher MK, Franck CM. Analysis of transient fault currents in multi-terminal HVDC networks during poleto-ground faults. International Conference on Power System Transients (IPST); 2013 Jul.
- 8. Asplund G, Erksson K, Jiang H, Lindberg J, Palsson R, Svensson K. DC transmission based on voltage source converters. Proc CIGRE SC 14 Colloq; South Africa; 1997.
- Jacobson B, Westman B, Bahrman MP. 500 kV VSC transmission system for lines and cables. Proc CIGRE, B4-6, San Francisco Colloq on Advances in Voltage Source Convertr (VSC) Technologies; 2012.
- Magg T, Manchen M, Krige E, Wasborg J, Sundin J. Connecting networks with VSC-HVDC in Africa: Caprivi link interconnector. IEEE PES PowerAfrica 2012 Conference and Exposition, South Africa; 2012 Jul. https:// doi.org/10.1109/PowerAfrica.2012.6498630
- Liu H, Xu Z, Huang Y. Study of protection strategy for VSC based HVDC system. Proc IEEE/PES T&D Conference; 2003 Sep. p. 49-54.
- Tang L, Ooi BT. Protection of VSC multi-terminal HVDC against DC faults. 33rd Annual IEEE Power Electronics Specialist Conference; 2002 Nov. p. 719-24.
- Tang L, Ooi BT. Locating and isolating DC faults in multi-terminal DC systems. IEEE Trans Power Del. 2007 Jul; 22(3):1877-84. https://doi.org/10.1109/ TPWRD.2007.899276
- Candelaria J, Park JD. VSC-HVDC system protection: A review of current methods. Proc IEEE/PES Power Systems Conference and Exposition (PSCE); 2011 Mar. https://doi. org/10.1109/PSCE.2011.5772604
- Franck CM. HVDC circuit breaker: A review identifying future research needs. IEEE Trans Power Del. 2011 Apr; 26(2):998 -1007. https://doi.org/10.1109/TPWRD.2010.2095889
- 16. Bucher MK, Walter MM, Pfeiffer M, Franck CM. Options for ground fault clearance in HVDC offshore networks. IEEE

Energy Conversion Congress and Exposition (ECCE); 2012. p. 2880-7. https://doi.org/10.1109/ECCE.2012.6342371

- Li X, Song Q, Liu W, Rao H, Xu S, Li L. Protection of nonpermanent faults on DC overhead lines in MMC-based HVDC systems. IEEE Trans Power Delivery. 2013 Jan; 28(1): 483-90. https://doi.org/10.1109/TPWRD.2012.2226249
- Xue Y, Xu Z. On the bipolar MMC-HVDC topology suitable for bulk power overhead line transmission: configuration, control, and dc fault analysis. IEEE Trans Power Delivery. 2014 Dec; 29(6):2420-9. https://doi.org/10.1109/ TPWRD.2014.2352313
- Sneath J, Rajapakse AD. Fault detection and interruption in an earthed HVDC grid using ROCOV and hybrid DC breakers. IEEE Trans Power Delivery. 2016; 31(3):973-81. https://doi.org/10.1109/TPWRD.2014.2364547
- Descloux J, Gandioli C, Raison B, Hadjsaid N, Tixador P. Protection system for meshed HVDC network using superconducting fault current limiters. IEEE Grenoble PowerTech; 2013 Jun. p. 1-5. https://doi.org/10.1109/ PTC.2013.6652389
- Schettler F, Huang H, Christl N. HVDC transmission systems using voltage sourced converters design and applications. IEEE Power Engineering Society Summer Meeting; 2000 Jul; 2:715-20.
- 22. Tang L, Ooi BT. Managing zero sequence in voltage source converter. Proc Ind Appl Soc Conf; 2002. p. 2186-92.
- 23. Tang L. Control and protection of multi-terminal DC transmission systems based on voltage-source converters [Ph.D Dissertation]. Canada: McGill University; 2003. p. 98-123.
- Yang J, Zheng J, Tang G, He Z. Characteristics and recovery performance of VSC-HVDC transmission line fault. Proc Power and Engineering Conference (APPEEC); 2010 Apr. p. 1-4. https://doi.org/10.1109/APPEEC.2010.5449063
- Hajian M, Jovcic D, Wu B. Evaluation of semiconductor based methods for fault isolation on high voltage DC grids. IEEE Trans Smart Grid. 2013 Jun; 4(2):1171-9. https://doi. org/10.1109/TSG.2013.2238260
- 26. Chaudhary SK, Teodorescu R, Rodrriguez P, Kjar PC. Chopper controlled resistors in VSC-HVDC transmission for WPP with full scale converters. IEEE PES/IAS Conf on Sustainable Alternative Energy (SAE); Denmark. 2009. p. 1-8. https://doi.org/10.1109/SAE.2009.5534882 PMCid:PMC2667167
- Callavik M, Blomberg A, Hafner J, Jacobson B. The hybrid HVDC breaker-An innovation breakthrough enabling reliable HVDC grids [ABB Grid Systems Technical Paper]; 2012 Nov.
- Manohar P, Ahmed W. Superconducting fault current limiter to mitigate the effect of DC line fault in VSC-HVDC system. International Conference on Power, Signals, Control and Computations (EPSCICON-2012), India; 2012 Jan 3-6. p. 1-6. ISBN: 978-1-4673-0446-7.

- Ahmed W, Manohar P. DC line protection for VSC-HVDC system. IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES 2012), India; 2012 Dec 16-19. ISBN:978-1-4673-4506-4. https:// doi.org/10.1109/PEDES.2012.6484499
- Manohar P, Ahmed W. Application of superconducting fault current limiter in multi-terminal HVDC systems. Proc CIGRE, HVDC and Power Electronics International Colloquium, India; 2015 Sep. p. 297-311.
- Noe M, Steurer M. High temperature superconductor fault current limiters: concepts, applications and development status. Superconducting Sci Technology. 2007; 20:R15-R29. https://doi.org/10.1088/0953-2048/20/3/R01
- 32. Sokolovsky V, Meerovich V, Vajda I, Beilin V. Superconducting FCL: design and application. IEEE Trans App Superconductivity. 2004 Sep; 14(3):1990-9. https://doi. org/10.1109/TASC.2004.830608
- CIGRE WG A3.16, Fault current limiters-application, principles and experience. CIGRE SC A3 and B3 Joint Colloq; Tokyo; 2005.
- 34. Paul W, Chen M, Lakner M, Rhyner J, Braun D, Lanz W, Kleimaier M. Superconducting fault current limiter-applications, technical and economical benefits, simulations and test results. Proc. 13-201 CIGRE Session; Paris, France; 2000.
- 35. Langston J, Steurer M, Woodruff S, Baldwin T, Tang J. A generic real time computer simulation model for superconducting fault current limiters and its applications in system protection studies. IEEE Trans App Superconductivity. 2005 Jun; 15(2):2090-3. https://doi.org/10.1109/ TASC.2005.849459
- 36. Noe M, Kudymow A, Fink S, Elschner S, Breuer F, Bock J, Walter H, et al. Conceptual design of a 110 kV resistive superconducting fault current limiter using MCP-BSCCO 2212 bulk material. IEEE Trans App Supercond. 2007 Jun; 17(2). https://doi.org/10.1109/TASC.2007.898125
- 37. Yuan X, Tekletsadik K, Kovalsky L, Bock J, Breurer F, Elschner S. Proof of concept prototype test results of a Superconducting fault current limiter for transmission level applications. IEEE Trans App. Supercond. 2005 Jun; 15(2):1982-5. https://doi.org/10.1109/TASC.2005.849432
- Tekletsadik K. High volatge design for a 138 kV superconducting fault current limiter. Proc IEEE-CEDIP 2005 Workshop on Cryogenics Dielectrics; 2005 Oct.
- Polasek A, Dias R, Serra ET, Filho OO, Niedu. Short circuit testing of monofilar Bi-2212 coils connected in series and in parallel. Jour Physics, EUCAS 09; 2010. p. 1-11. https:// doi.org/10.1088/1742-6596/234/3/032048
- 40. Kraemer H, Schmidt W, Utz B, Wacker B, Neumueller HW, Ahlf G, Hartig R. Test of 1 kA superconducting fault current limiter for DC applications. IEEE Trans App Supercond. 2005 Jun; 15(2):1986-9. https://doi.org/10.1109/ TASC.2005.849433

- 41. Tixador P, Villard C, Cointe Y. DC superconducting fault current limiter. Supercond Sci Tech. 2006 Feb; S118-S125. https://doi.org/10.1088/0953-2048/19/3/017
- Cointe Y, Tixador P, Villard C. FCL: A solution to fault current problems in DC networks. 8th European Conference on Applied Superconductivity (EUCAS 2007), Journal of Physics. 2008; 97:1-8. https://doi.org/10.1088/1742-6596/97/1/012062
- Chen Y, Liu X, Sheng J, Cai L, Jin Z, Gu J, An Z, Yang X, Hong Z. Design and application of superconducting fault current limiter in DC systems. IEEE Trans App. Supercond. 2014 Jun; 24(3). https://doi.org/10.1109/TASC.2013.2284936
- 44. Ye L, Juengst KP. Modeling and simulation of high temperature resistive superconducting fault current limiters.

IEEE Trans App Superconductivity. 2004 Jun; 14(2):839-42. https://doi.org/10.1109/TASC.2004.830293

- 45. Steurer M, Brechna H, Frohlich K. A nitrogen gas cooled, hybrid, high temperature superconducting fault current limiter. IEEE Trans App Supercond. 2000 Mar; 10(1):840-4. https://doi.org/10.1109/77.828362
- Du C, Agneholm E, Olsson G. Comparison of different frequency controllers for a VSC-HVDC supplied system. IEEE Trans Power Delivery. 2008 Oct; 23(4):2224-32. https://doi. org/10.1109/TPWRD.2008.921130
- 47. Li G, Yin M, Zhou M, Zhao C. Modeling of VSC-HVDC and control strategies for supplying both active and passive systems. IEEE Power Engineering Society General Meeting; Montreal, Que; 2006. p. 1-6.