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Admittance based algorithm of dynamic voltage restorer for improved power quality

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Abstract:This study deals with the admittance estimation algorithm for DVR for improvement of PQ in PDS (Power Distribution System). This admittance estimation algorithm based DVR is simple and easy to implement in simulation/hardware. In this admittance estimation algorithm, the estimation of active/reactive power components of load voltages are based on unit vectors in time domain and Low-Pass Filter (LPF). The mathematical analysis is easy, accurate and is used for fast estimation of reference load voltages using proposed algorithm. A three phase DVR using admittance estimation algorithm is modeled and implemented on real time hardware under balanced/unbalanced voltage sag, balanced/unbalanced voltage swell and harmonics compensation using Real Time Hardware Simulation and MATLAB under Simulink. Performance of admittance estimation algorithm for DVR in PDS shows quite satisfactory results using RT-LAB and MATLAB for the above power quality problems as per IEC and IEEE standards.

Index Terms: *DVR, harmonics, admittance estimation algorithm, voltage sag/swell, distribution System*

1.0 INTRODUCTION

The power quality (PQ) is an one of the key area of research in electrical engineering mostly in distribution and utilization system [1]. The main attention has been concentrated towards PQ issues caused by linear/non-linear loads and nonlinear ac mains. Generally the non-linear loads due to power converters used in paper, refrigeration, textile, cement and transportation industries [2,3]. Series active line conditioners are used for compensation of voltage-based distortions such as voltage sag/swell, harmonics and unbalanced voltage sag/swell etc. DVR is one of series active conditioners to mitigate voltage based PQ (Power Quality) Issues. The primary components of proposed DVR consists of injecting transformer, capacitor based VSC, ac inductor and ripple filter at injecting transformer. To mitigate PQ problems such as balanced sag/unbalanced sag, balanced swell/ unbalanced swell and harmonics are mitigated using capacitor based DVR [4].

The main purpose of proposed DVR is it injects voltage in 90o phase shift with supply current so that under steady state the active power required is zero. The prime disadvantage of capacitor supported DVR

under balanced/unbalanced voltage sag/swell is the voltage at load is not in phase with balanced/ unbalanced pre-voltage sag/swell. The balanced/ unbalanced pre-sag/swell compensation the proposed DVR will injects/absorbs required active power from distribution system [5]-[6].

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The design, protection and many topologies of DVR are discussed in literature [7]-[9]. To compensate voltage related PQ problems the capacitor supported DVR has to respond quickly for estimation of reference load voltages using control strategies. Different control algorithms for proposed DVR are Space Vector PWM Based Control Strategy [10], PQR Instantaneous Power Theory [11], Adaline Based Control Algorithm [12],ISCT (Instantaneous Symmetrical Components Theory) [13], SRFT (Synchronous Reference Frame Theory) [14] etc, These traditional control algorithms of DVR takes more time for estimation of reference load voltages.

This paper proposes admittance estimation algorithm for DVR to mitigate balanced voltage sag/unbalanced voltage sag, balanced voltage swell/unbalanced voltage swell, and harmonics. The proposed admittance estimation algorithm is simple, robust and takes less execution time for estimation of reference load voltages. The proposed admittance estimation algorithm based DVR is modeled in RT-LAB and MATLAB 2013b under Simulink & performance results are validated.

2.0 CONFIGURATION OF DVR AND CONTROL ALGORITHM

A three phase DVR based on VSC (Voltage Source Converter) is depicted in Fig.1, where three phase ac source impedance (Z_s) is feeding to three loads.

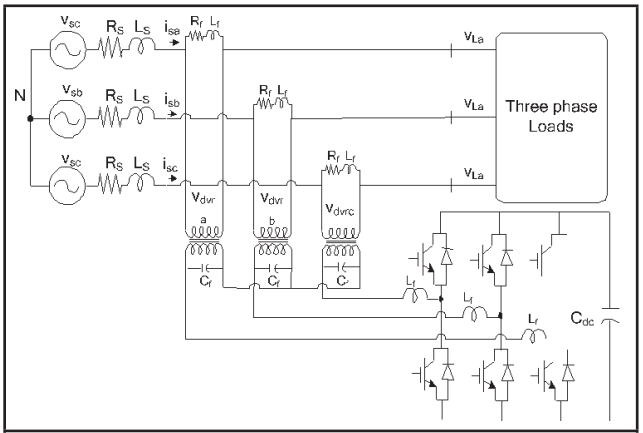

FIG.1 CAPACITOR BASED DVR IN DISTRIBUTION SYSTEM

The main required components for DVR are three phase VSC, injecting transformer, series connected ripple filter (R_f and C_f) and interfacing inductor (L_f). Fig.1 shows the three phase supply voltages (v_{sa},v_{sb},v_{sc}), per phase source currents (i_{sa}, i_{sb}, i_{sc}), per phase load voltages (v_{La},v_{Lb},v_{Lc}), injecting transformer voltages (v_{dvra},v_{dvrb},v_{dvrc}), dc bus voltage(v_{dc}) and terminal PCC voltage(v_t). Fig.2 shows diagram of admittance estimation control algorithm based DVR for estimation of reference load voltages (v_{La}^*,v_{Lb}^*,v_{Lc}^*).

2.1 Estimation of Direct and Quadrature Unit Templates

The instantaneous supply currents (i_{sa}, i_{sb}, i_{sc}) of distribution system having zero and negative sequence components, these supply currents are given LPFs (Low Pass Filters) to eliminate noise and harmonics.

The estimated magnitude of supply currents (i_{ta}, i_{tb}, i_{tc}) are determined by squaring instantaneous supply currents as follows

$$i_{ta} = \sqrt{2(\frac{i_{sa}^2}{3})}; i_{tb} = \sqrt{2(\frac{i_{sb}^2}{3})}; i_{tc} = \sqrt{2(\frac{i_{sc}^2}{3})}; \quad ...(1)$$

The total resultant magnitude of source current (i^{st}) is estimated from each phase source currents (i_{ta}, i_{tb}, i_{tc}) is given by

$$i_{st} = (i_{ta} + i_{tb} + i_{tc})/3 \quad ...(2)$$

The direct axis component unit-templates (u_{das}, u_{dbs}, u_{dcs}) of three phase supply currents are estimated as

$$u_{das} = \frac{i_{sa}}{i_{st}}; u_{dbs} = \frac{i_{sb}}{i_{st}}; u_{dcs} = \frac{i_{sc}}{i_{st}}; \quad (3)$$

The dc bus error (V_{dce}) is the difference of reference dc bus voltage (v_{dc}^*) and sensed magnitude of dc bus voltage (v_{dc}) of VSC at rth sampling instant is estimated as,

$$v_{dce(r)} = -v_{dc(r)} + v_{dc}^{*}{}_{(r)} \quad ...(4)$$

The output voltage error at DC bus (v_{dce}) is feeding to DC bus PI controller and this output(plsd) is

required to regulate DC bus voltage of DVR at r[th] sampling instant is given as

$$p_{lsd(r)} = p_{lsd(r-1)} + k_{dp}(v_{dce(r)} - v_{dce(r-1)}) + k_{di}v_{dce(r)} \quad ...(5)$$

Where vdce (r) and vdce (r-1) are output voltage error in the DC bus voltage at rth and (r-1) [th] sample instants and kdp and kdi are DC bus PI gain constants. The $P_{lsd(k)}$ is taken as loss component of supply power.

The P_{lsd} corresponding loss conductance (G_{lsd}) is estimated as,

$$G_{lsd} = p_{lsd} / \left[v_{st}^2 \left\{ \left(u_{das}^2 + u_{dbs}^2 + u_{dcs}^2 \right) \right\} \right] \quad ...(6)$$

The three phase instantaneous active load power (p_L) is estimated as

$$p_L = p_{Lac} + p_{Ldc} = \left\{ v_{st} \left(u_{das} i_{sa} + u_{dbs} i_{sb} + u_{dcs} i_{sc} \right) \right\} \quad ...(7)$$

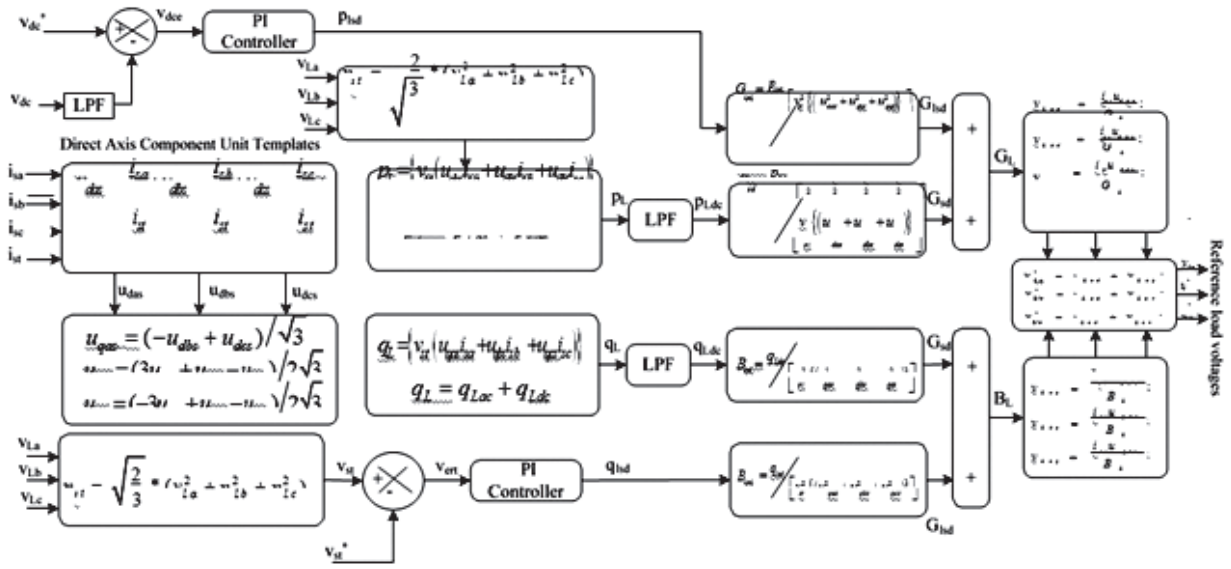

FIG.2. REFERENCE VOLTAGES USING ADMITTANCE ESTIMATION ALGORITHM

A LPF (Low Pass Filter) is used for extraction of the dc component active power (P_{Ldc}) from active load power (p_L).

The fundamental source voltage corresponding conductance (Gsd) is estimated as

$$G_{sd} = p_{Ldc} / \left[v_{st}^2 \left\{ \left(u_{das}^2 + u_{dbs}^2 + u_{dcs}^2 \right) \right\} \right] \quad ...(8)$$

The direct-axis components of reference load voltages (v_{Lad}, v_{Lbd} , v_{Lcd}) are estimated as,

$$v_{Lad} = \frac{i_{st} u_{das}}{G_L}; v_{Lbd} = \frac{i_{st} u_{dbs}}{G_L}; \; v_{Lcd} = \frac{i_{st} u_{dcs}}{G_L}; \quad ...(9)$$

The quadrature axis unit-templates (u_{qas}, u_{qbs}, u_{qcs}) of three phase supply currents are estimated as

$$u_{qas} = (-u_{dbs} + u_{dcs}) / \sqrt{3} \quad ...(10)$$

$$u_{qbs} = (3u_{das} + u_{dbs} - u_{dcs}) / 2\sqrt{3} \quad ...(11)$$

$$u_{qcs} = (-3u_{das} + u_{dbs} - u_{dcs}) / 2\sqrt{3} \quad ...(12)$$

The terminal voltage error (V_{ert}) is the difference of reference ac bus terminal voltage (v_{st}^*) and sensed magnitude of ac terminal voltage (v_{st}) at r[th] sampling instant is estimated as,

$$v_{ert} = v^*_{st(r)} - v_{st(r)} \quad ...(13)$$

The output voltage error at AC bus (v^{ert}) is feeding AC bus PI controller and this output (q_{lsd}) is required to regulate AC bus voltage of DVR at r sampling instant is given as

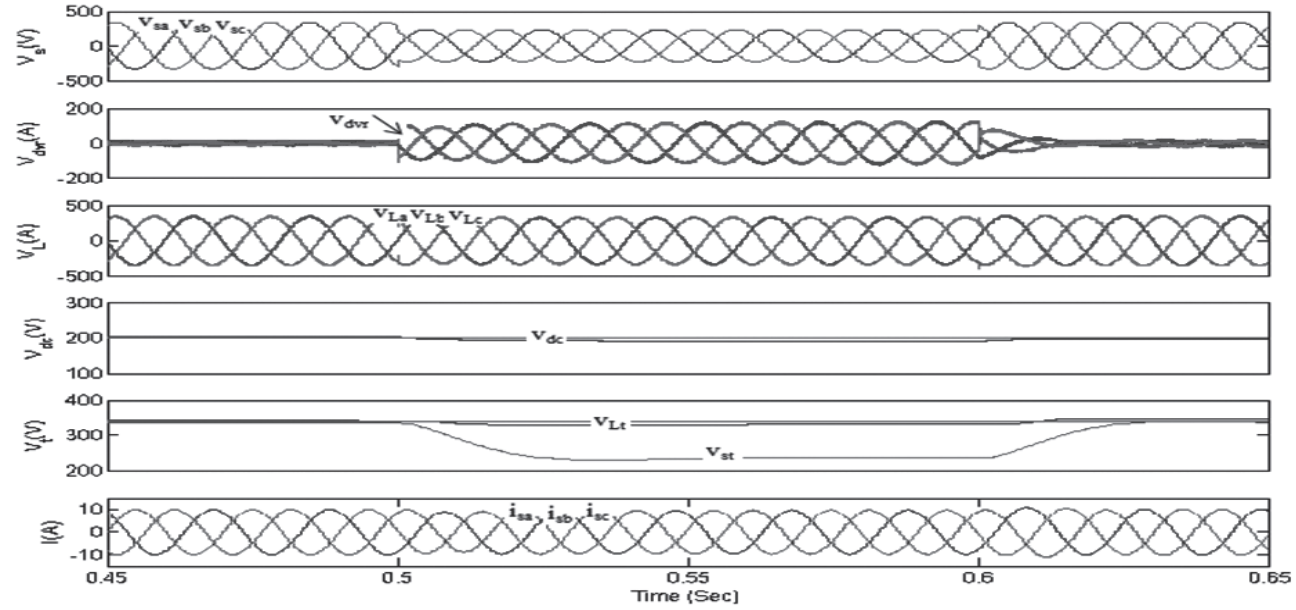

FIG.3 PERFORMANCE OF ADMITTANCE ESTIMATION ALGORITHM BASED DVR FOR 30% BALANCED VOLTAGE SAG

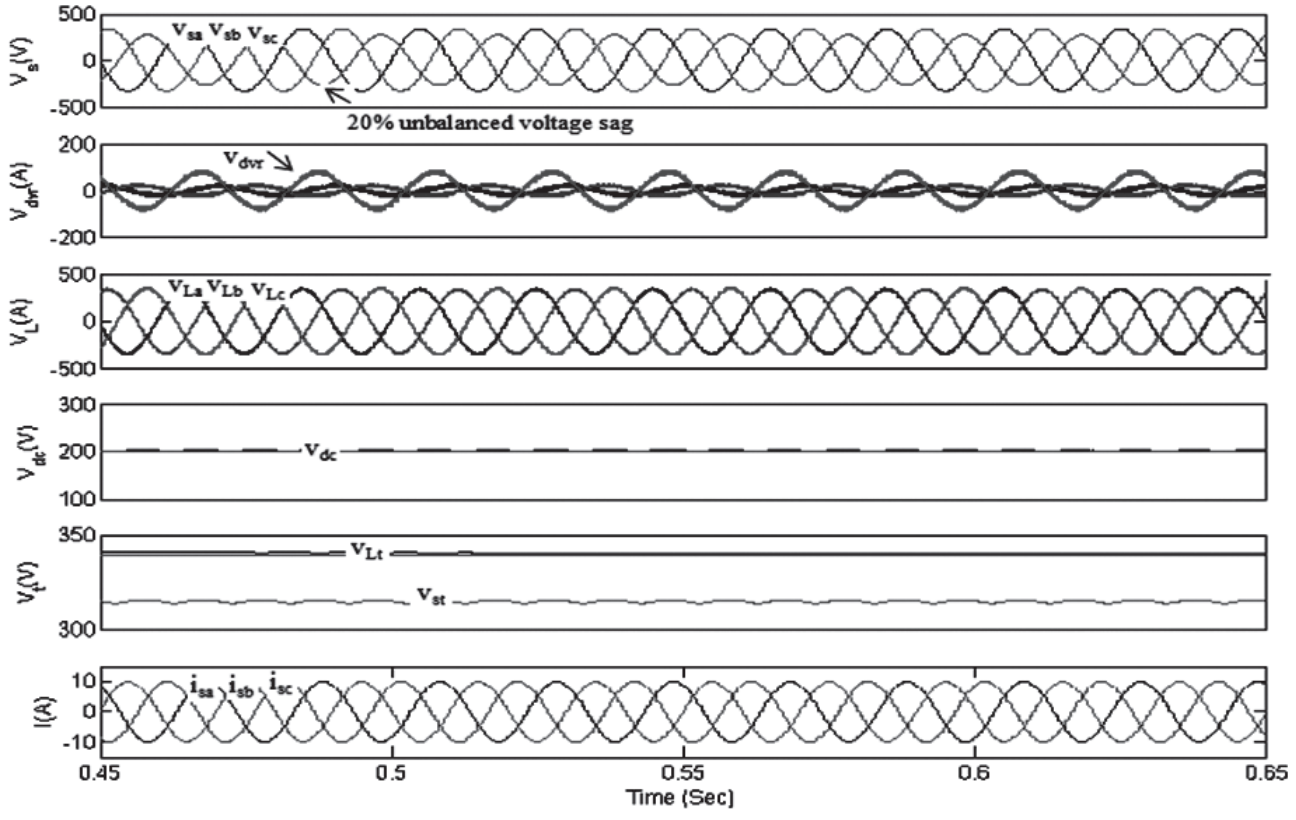

FIG.4 PERFORMANCE OF ADMITTANCE ESTIMATION ALGORITHM BASED DVR FOR 20% UNBALANCED VOLTAGE SAG IN ONE PHASE

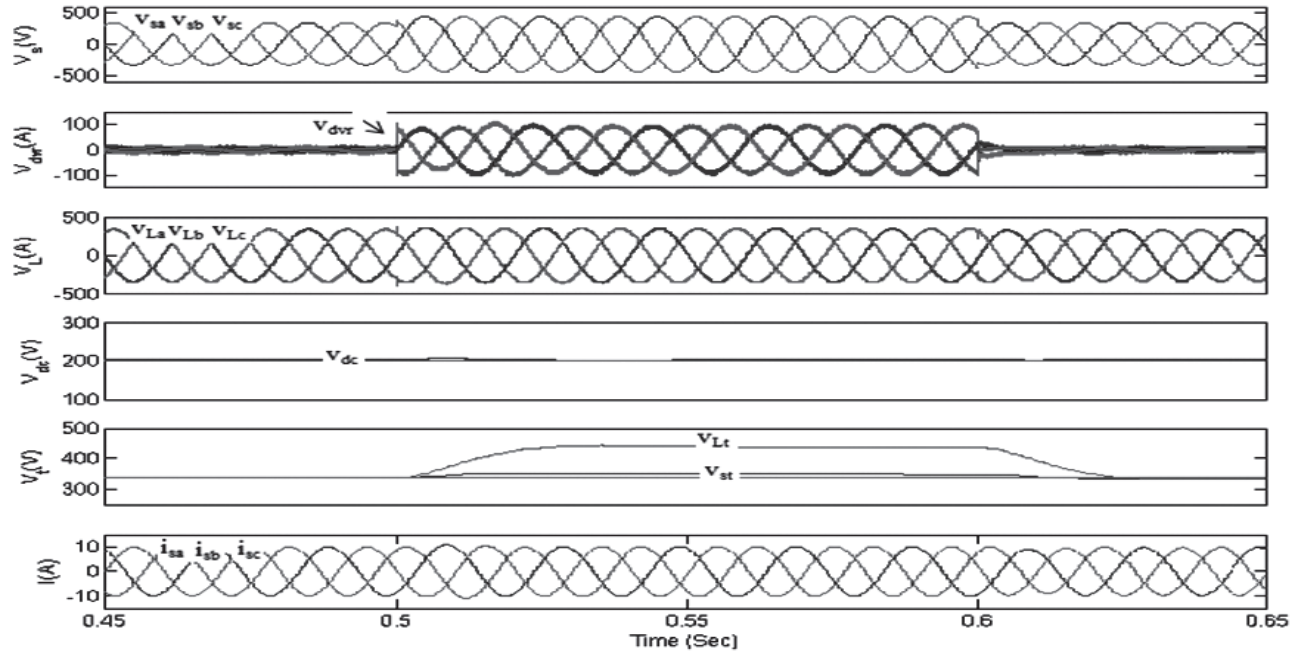

FIG.5 PERFORMANCE OF ADMITTANCE ESTIMATION ALGORITHM BASED DVR FOR 30% BALANCED VOLTAGE SWELL

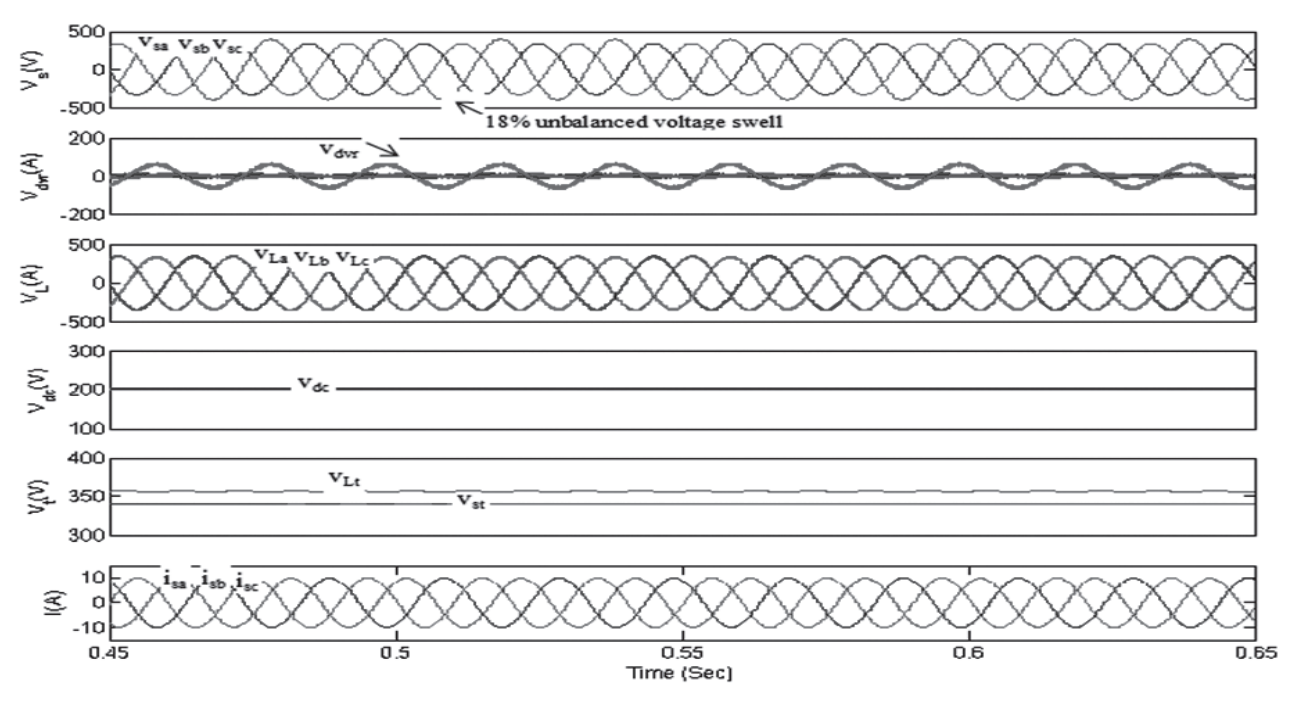

FIG.6 PERFORMANCE OF ADMITTANCE ESTIMATION ALGORITHM BASED DVR FOR 20% UNBALANCED VOLTAGE SWELL IN ONE PHASE

$$q_{lsd(r)} = q_{lsd(r-1)} + K_{qp}(v_{ert(r)} - v_{ert(r-1)}) + K_{qi} v_{ert(r)} \quad (14)$$

Where vert (r) and vert (r-1) are the output voltage error in the AC bus voltage at rth and (r-1)th sample instants and K_{qp} and K_{qi} are AC bus PI gain constants. The $q_{lsd(r)}$ is taken as loss component of supply power.

The sensed magnitude of AC bus terminal voltage (v_{st}) is estimated as

$$v_{st} = \sqrt{\frac{2}{3}} * (v_{La}^2 + v_{Lb}^2 + v_{Lc}^2) \quad ...(15)$$

The q_{lsd} corresponding loss susceptance (Blsd) is estimated as,

$$B_{lsd} = q_{lsd} / \left[v_{st}^2 \left\{ \left(u_{qas}^2 + u_{qbs}^2 + u_{qcs}^2 \right) \right\} \right] \quad ...(16)$$

The three phase instantaneous reactive load power (q_L) is estimated as

$$q_L = q_{Lac} + q_{Ldc} = \left\{ v_{st} \left(u_{qas} i_{sa} + u_{qbs} i_{sb} + u_{qcs} i_{sc} \right) \right\} \quad ...(17)$$

A LPF is used for extraction of the dc component reactive power (q_{Ldc}) from reactive load power (q_L). The fundamental source voltage corresponding susceptance (B_{sd}) is estimated as

$$B_{sd} = q_{Ldc} / \left[v_{st}^2 \left\{ \left(u_{qas}^2 + u_{qbs}^2 + u_{qcs}^2 \right) \right\} \right] \quad ...(18)$$

The total susceptance (B_L) of the distribution load is sum of loss admittance (B_{lsd}) and fundamental source admittance (B_{sd})

$$B_L = B_{lsd} + B_{sd} \quad ...(19)$$

The quadrature axis components of reference load voltages (vLaq, vLbq, vLcq) are estimated as,

$$v_{Laq} = \frac{i_{st} u_{qas}}{B_L}; v_{Lbq} = \frac{i_{st} u_{qbs}}{B_L}; \; v_{Lcq} = \frac{i_{st} u_{qcs}}{B_L}; \quad ...(20)$$

The reference load voltages (V_{La}^*, V_{Lb}^*, V_{Lc}^*) are estimated as,

$$v_{La}^* = v_{Lad} + v_{Laq}; v_{Lb}^* = v_{Lbd} + v_{Lbq}; v_{Lc}^* = v_{Lcd} + v_{Lcq}; \quad ...(21)$$

These reference load voltages (v_{La}^*, v_{Lb}^*, v_{Lc}^*) are La Lb Lc compared with sensed load voltages (v_{La}, v_{Lb}, v_{Lc}) in current controller.

These error voltages are given to PWM controller to generate switching signals for VSC.

3.0 SIMULATION MODELING

MATLAB based simulation models of Admittance Estimation Algorithm based DVR in three phase distribution system is developed to simulate their dynamic performance for validating control algorithm for various PQ problems. The proposed distribution system consists of three phase source, VSC based DVR, injecting transformer, ripple filer and admittance estimation control algorithm. To demonstrate performance of admittance estimation control algorithm based DVR, the linear/ nonlinear loads are considered. The MATLAB simulations are analyzed in discrete mode at 5e-6 fixed step size with ode23tb (stiff/ TR-BDF2) solver.

4.0 SIMULATION RESULTS AND DISCUSSION

In this investigation, power quality problems such as voltage harmonics, balance/unbalanced voltage sag, balanced/unbalanced voltage swell are demonstrated to verify admittance estimation algorithm based DVR for satisfactory results. The dynamic performance analysis of admittance estimation algorithm based DVR is simulated for voltage harmonics, balance/unbalanced voltage sag, balanced/unbalanced voltage swell for linear/ non- linear loads. The performance waveforms of admittance estimation algorithm based DVR are observed and gives satisfactory results at different PQ problems.

4.1 Performance of Admittance Estimation Algorithm based DVRoperation under Balanced Voltage Sag/Unbalanced Voltage Sag

The performance of DVR based on Admittance Estimation Algorithm during balanced voltage sag/unbalanced voltage sag at linear load is depicted in Fig.3-Fig.4. The dynamic performance indices of Admittance Estimation Algorithm based DVR are supply voltage (v_s), DVR compensating voltage (v_{dvr}), load voltage (v_L), source current(i_s), DC bus voltage(v_{dc}), terminal voltage(v_t), source current(i_L) are shown in Fig.3-Fig.4 for balanced voltage sag/unbalanced voltage sag during t= 0.45sec to 0.65sec. Fig.3 shows, at t=0.45 to 0.5sec and t=0.6 to 0.65sec, the source voltage (v_s), source current (i_s), load voltage(v_L) are highly balanced, purely sinusoidal and harmonic free. It is also observed from Fig.3 that when 30% of voltage sag was created at the source between t=0.5 to 0.6sec, the performance

of Admittance Estimation Algorithm based DVR injecting voltage (v_{dvr}) injecting such a way that the source current(i_s), load voltage(v_L) are highly balanced in simulation. Fig.4 shows, At t=0.45 to 0.65 sec one of phase is reduced by 20% but other two phases are maintained at rated value. It is observed from Fig.4, Admittance Estimation Algorithm based DVR injecting voltage (v_{dvr}) injecting such that the source current(i_s), load voltage(v_L) are highly balanced and harmonic free even when one of phase voltage reduced by 20%. Fig.3-Fig.4 shows the terminal voltage and DC bus voltage are maintained at 339V and 200V using Admittance Estimation Algorithm based DVR during balanced voltage sag/unbalanced voltage sag. The performance waveforms of fig.3 and fig.4 are shows satisfactory results for balanced voltage sag/unbalanced voltage sag in simulation.

4.2 Performance of Admittance Estimation Algorithm based DVR Operation under Balanced Voltage Swell/Unbalanced Voltage Swell

The performance of DVR based on Admittance Estimation Algorithm during balanced voltage swell/unbalanced voltage swell at linear load is depicted in Fig.5-Fig.6. The dynamic performance indices of Admittance Estimation Algorithm based DVR are supply voltage (vs), DVR compensating voltage (vdvr), load voltage (vL), DC bus voltage(vdc), terminal voltage(vt), source current(iL) are shown in Fig.5-Fig.6 for balanced voltage swell/unbalanced voltage swell during t= 0.45sec to 0.65sec. Fig.5 shows, at t=0.45 to 0.5sec and t=0.6

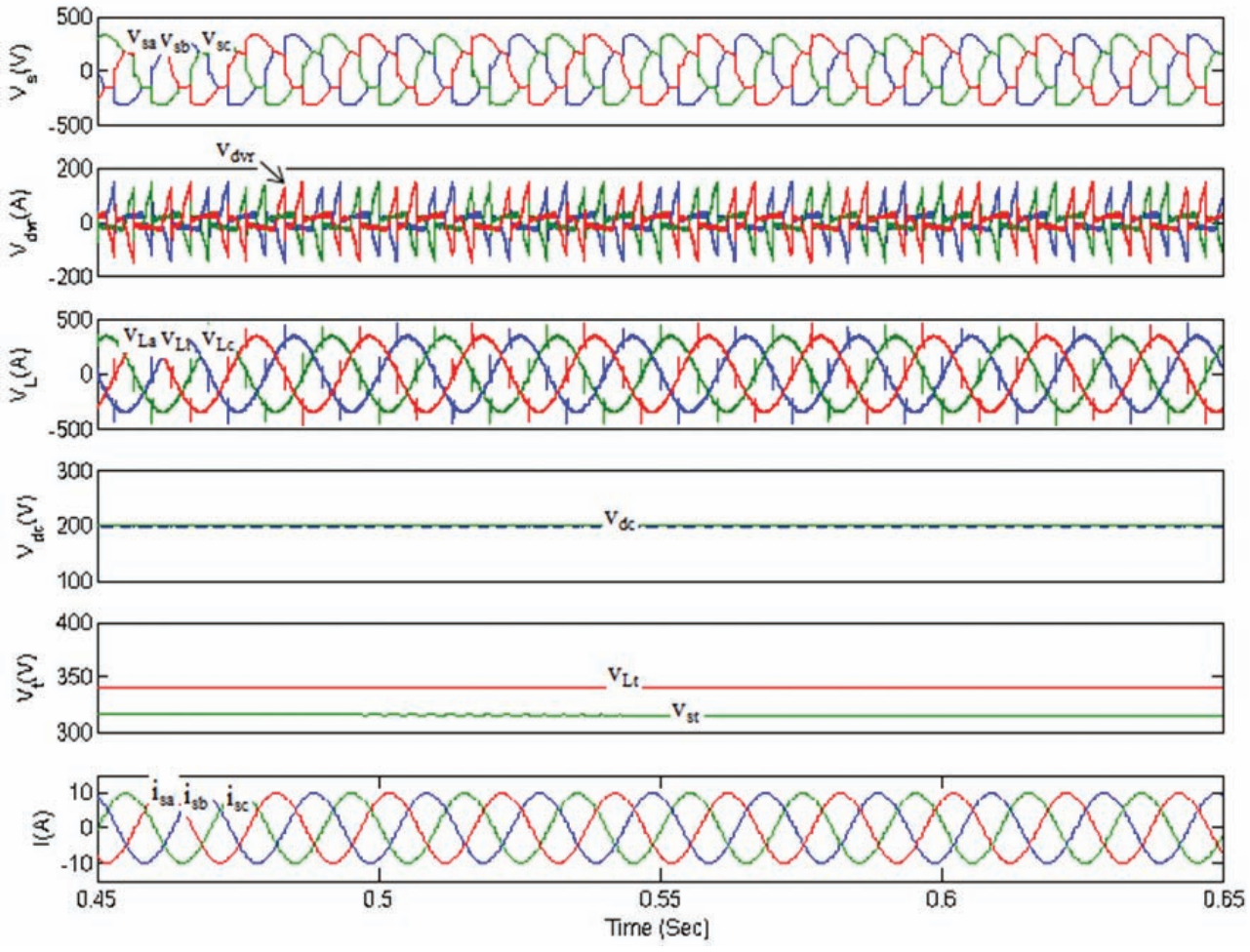

FIG.7 PERFORMANCE OF ADMITTANCE ESTIMATION ALGORITHM BASED DVR UNDER HARMONIC MITIGATION

to 0.65sec, the source voltage(v_s), source current(i_s), load voltage(v_L) are highly balanced, purely sinusoidal and harmonic free in simulation.

It is also observed from Fig.6 that when 30% of voltage swell was created at the source between t=0.5 to 0.6sec, the performance of Admittance Estimation Algorithm based DVR injecting voltage (v_{dvr}) injecting such a way that the source current(is), load voltage(v_L) are highly balanced.

Fig.6 shows, At t=0.45 to 0.65 sec one of phase is increased by 18% but other two phases are maintained at rated value. It is observed from Fig.6, Admittance Estimation Algorithm based DVR injecting voltage (v_{dvr}) injecting such a way that the source current(i_s), load voltage(v_L) are highly balanced and harmonic free even when one of phase voltage increased by 18%. Fig.5-Fig.6 shows the terminal voltage and DC bus voltage are maintained at 339V and 200V using Admittance Estimation Algorithm based DVR during balanced voltage swell/unbalanced voltage swell. The performance waveforms of fig.5 and fig.6 are shows satisfactory results for balanced voltage swell/unbalanced voltage swell in simulation.

4.3 Performance of Admittance Estimation Algorithm based DVR Operation During Harmonics Mitigation

The performance of DVR based on Admittance Estimation Algorithm during harmonics mitigation under non-linear load is depicted in Fig.7. The dynamic performance indices of Admittance Estimation Algorithm based DVR are supply voltage (v_s), DVR compensating voltage (v_{dvr}), load voltage (v_L), DC bus voltage(v_{dc}), terminal voltage(v_t), source current (i_s) are shown in Fig.7 under harmonic mitigation. During t= 0.45 to 0.65sec, Admittance Estimation Algorithm based DVR injecting in such a way that load voltage (v_L) and source current (i_s) are highly balanced and harmonic free even though source voltage(v_s) has high harmonic content. Fig.7 shows the terminal voltage and DC bus voltage are maintained at 339V and 200V using Admittance Estimation Algorithm based DVR during harmonic mitigation. The performance indices of Admittance Estimation Algorithm based DVR are source has voltage (v_s) of 241.4 V and its THD of 8.9%,whereas the load has voltage (vL) of 238.2V and its THD of 3.50% are shown in Fig.8(a)-Fig.8(b).

5.0 REAL TIME IMPLEMENTATION

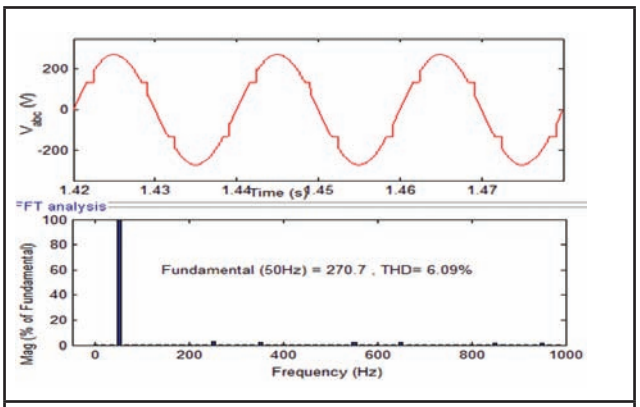

FIG.8 (A) SOURCE VOLTAGE (VS) HARMONIC SPECTRA IN SIMULATION

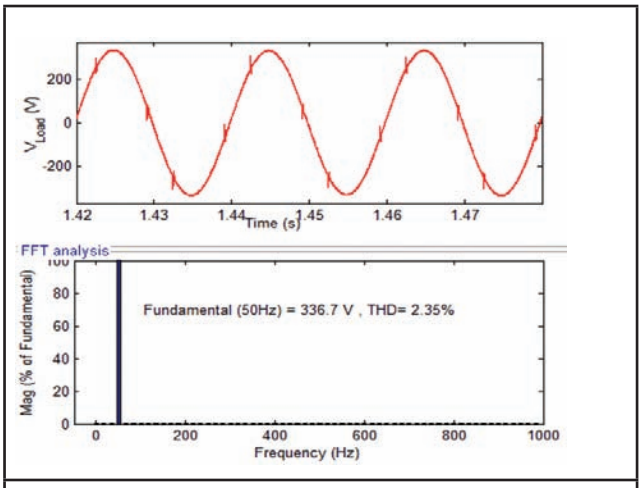

FIG.8 (B). LOAD VOLTAGE (VL) HARMONIC SPECTRA IN SIMULATION

A prototype 100kW 415V 50-Hz Y-connected source and distribution load along with admittance estimation algorithm based DVR is developed and implemented in real time. A diode universal with R- L load is taken as consumer loads to demonstrate harmonic compensation. Distribution load is taken as balanced R-L load. The admittance estimation control algorithm based DVR is modeled and implemented in real time with fixed step size of 40μs and

ODE4 (Runge-Kutta) solver. A three leg IGBT-based VSC is used as DVR for a 100KW 415V 50Hz Y-connected system at PCC through injecting transformer and inductor filter. A dc bus capacitor value of 3000μF is used and is regulated at 200 V. Performance parameters are recorded using a Fluke 43B power analyzer.

6.0 EXPERIMENTAL RESULTS AND DISCUSSION

The real time hardware results of Admittance Estimation Algorithm based DVR under balanced voltage sag/unbalanced voltage sag, balanced voltage swell/unbalanced voltage swell harmonics compensation are shown in Fig.9-Fig.13. The parameters indices of distribution system such as supply voltage of 'a' phase (v_{sa}), compensating voltage (v_{dvr}), load voltage of 'a' phase (v_L), dc bus voltage(v_{dc}), source terminal voltage(vst), load terminal voltage(v_{Lt}) are shown in Fig.9-Fig.13.

6.1 Experimental results of Admittance Estimation Algorithm based DVR under Balanced Voltage Sag /Unbalanced Voltage Sag

The hardware results of DVR on Admittance Estimation Algorithm during balanced voltage sag and unbalanced voltage sag are depicted in Fig.9 and Fig.10. A 30% of balanced voltage sag is introduced in linear load condition. When source voltage (v_{sa}) of 216.9V, the proposed Admittance Estimation Algorithm based DVR injects compensating voltage (v_{dvr}) such that load voltage (v_{La}) are highly balanced, sinusoidal and maintains at voltage of 238.7V. The dc bus voltage (v_{dc}) of Admittance Estimation Algorithm based DVR is maintained at 194.2V under balanced voltage sag is shown in Fig.9. The source terminal voltage (v_{st}) and load terminal voltage (v_{Lt}) are maintained at 300.3V and 330.9V in the real time hardware.

Under unbalanced voltage condition, A 20% reduced voltage in 'c' phase is introduced compared to 'a' and 'b' phases under linear load condition. The proposed Admittance Estimation Algorithm based DVR injects compensating voltage (vdvr) in such a way that load voltage (v_{La}) are purely sinusoidal, highly balanced. It was observed that from fig.10 that dc bus voltage (v_{dc}) is maintained at 195.24V in the real time hardware.

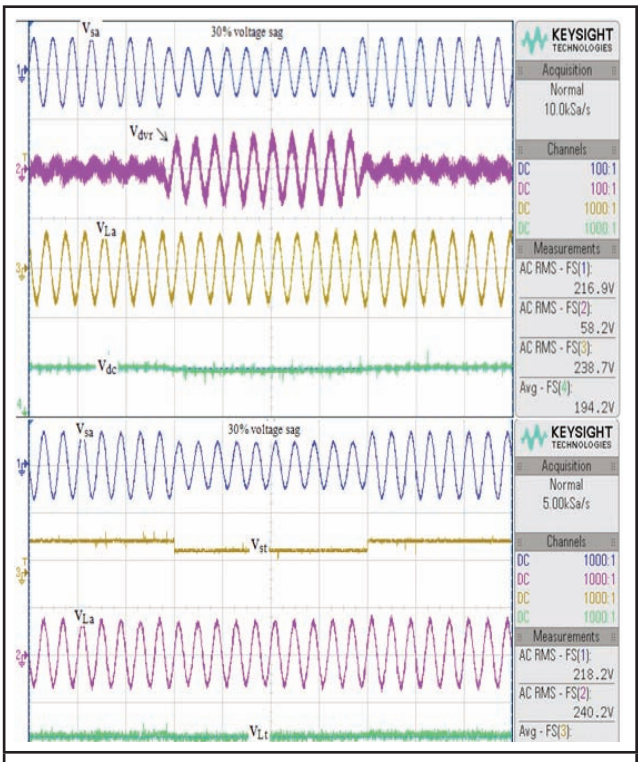

FIG.9 HARDWARE SIMULATION OF ADMITTANCE ESTIMATION ALGORITHM BASED DVR FOR 30% BALANCED VOLTAGE SAG

6.2 Experimental Results of Admittance Estimation Algorithm based DVR under Voltage Swell

The hardware results of DVR on Admittance Estimation Algorithm during balanced voltage swell and unbalanced voltage swell are depicted in Fig.11 and Fig.12. A 30% of balanced voltage swell is introduced in linear load condition. When source voltage (v_{sa}) of 274.8V, the proposed Admittance Estimation Algorithm based DVR injects compensating voltage (v_{dvr}) such that load voltage (v_{La}) are highly balanced, sinusoidal and maintains at voltage of 240.1V. The dc bus voltage (v_{dc}) of Admittance Estimation Algorithm based DVR is maintained at 202.1V under balanced voltage sag is shown in Fig.11. The

source terminal voltage (vst) and load terminal voltage (v_{Lt}) are maintained at 382.2V and 334.6V in the real time hardware.

Under unbalanced voltage condition, A 20% increase voltage in 'c' phase is introduced compared to 'a' and 'b' phases under linear load condition. The proposed Admittance Estimation Algorithm based DVR injects compensating voltage (v_{dvr}) in such a way that load voltage (v_{La}) are purely sinusoidal, highly balanced. It was observed that from fig.12 that dc bus voltage (v_{dc}) is maintained at 196.21V in the real time hardware.

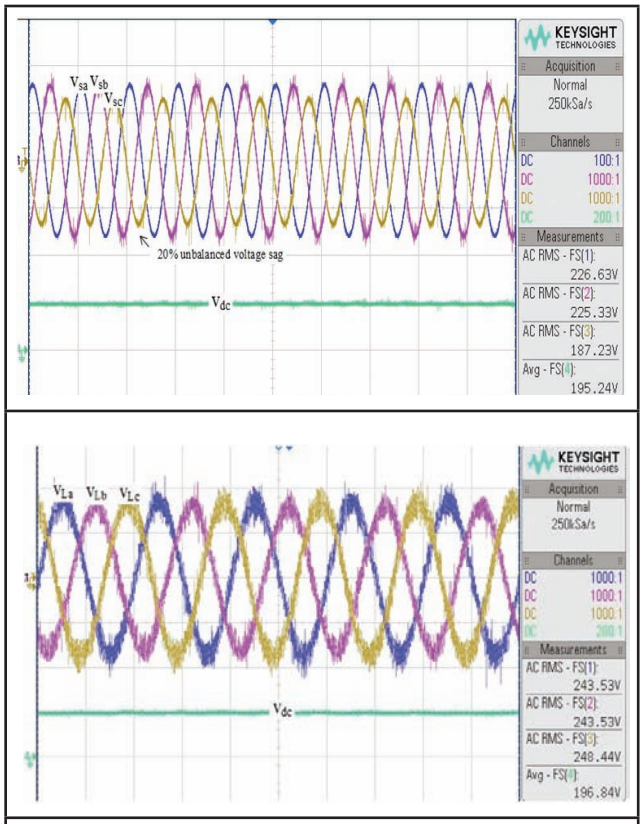

FIG.10 HARDWARE SIMULATION OF ADMITTANCE ESTIMATION ALGORITHM BASED DVR FOR 20% UNBALANCED VOLTAGE SAG

6.3 Hardware Results of Admittance Estimation Algorithm based DVR under Harmonics Compensation

The hardware results of DVR on Admittance Estimation Algorithm during harmonics compensation at non-linear load is depicted in Fig.13. A highly non-linear load is connected at distribution load to demonstrate harmonics compensation. The proposed admittance estimation algorithm based DVR injects compensating voltage(v_{dvr}) in such a way that load voltage (v_{La}) are purely sinusoidal, harmonic free and it maintains at voltage of 238.5V. It was observed that from fig.13 that dc bus voltage (v) is maintained at 198.91V in the real time hardware. Fluke 43B power analyzer is used to demonstrate %THD of source voltage and load voltage. The source voltage of %THD of 8.9% and its fundamental voltage of 240.1V whereas load voltage of %THD of 3.5% and its fundamental voltage of 238.2V are shown in Fig.14(a)- Fig.14(b).

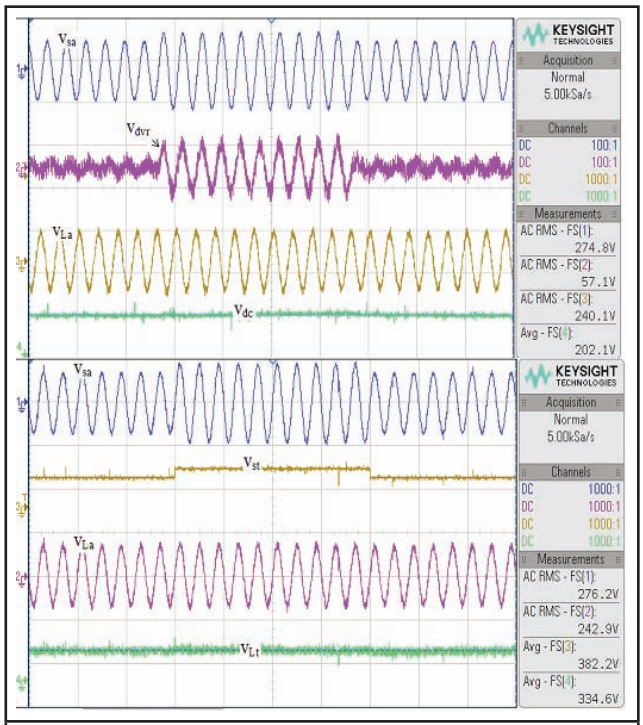

FIG.11 HARDWARE SIMULATION OF ADMITTANCE ESTIMATION ALGORITHM BASED DVR FOR 30% BALANCED VOLTAGE SWELL

7.0 CONCLUSION

The proposed paper improves PQ in distribution system using Admittance Estimation Algorithm based DVR. This proposed DVR is modeled, designed and developed in RT-LAB and MATLAB/SIMULINK, it consists of three-leg VSC, admittance estimation algorithm, linear/ non- linear load, ripple filter, injecting transformer. Performance of DVR primarily depends on

control algorithms to extract reference load voltages for regulating terminal voltage and dc bus voltage along with PQ improvement. For extracting reference load voltages, some new and modified control algorithms are used such as SRF, IRPT, PBT, ISCT, IcosΦ, Adaline and single phase pq theory. The admittance estimation algorithm is more stable to mitigate PQ problems compared above algorithms. This paper proposes admittance estimation algorithm based DVR shows satisfactory simulation and hardware results under load fluctuations for various PQ problems as per IEC and IEEE standard.

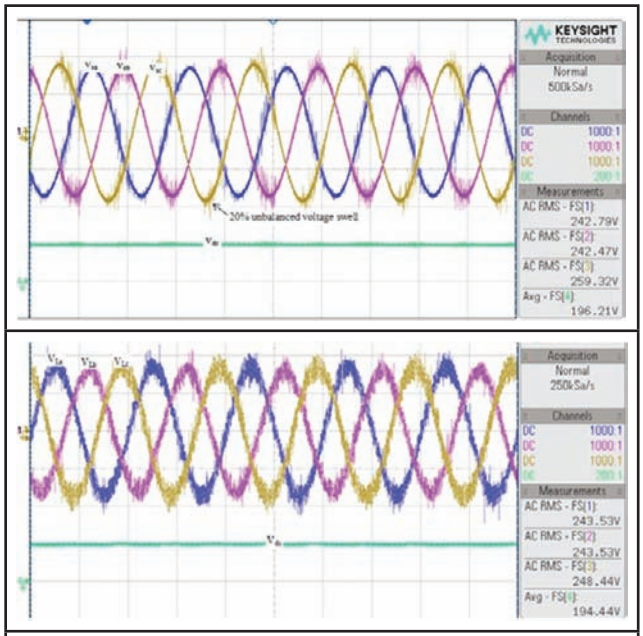

FIG.12 HARDWARE SIMULATION OF ADMITTANCE ESTIMATION ALGORITHM BASED DVR FOR 20% UNBALANCED VOLTAGE SWELL

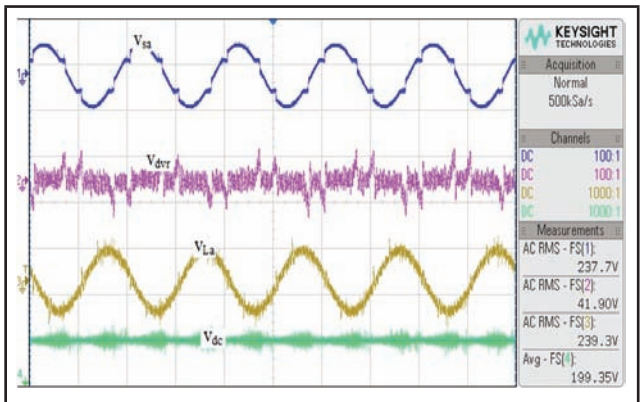

FIG.13 HARDWARE SIMULATION OF ADMITTANCE ESTIMATION ALGORITHM BASED DVR UNDER HARMONIC MITIGATION

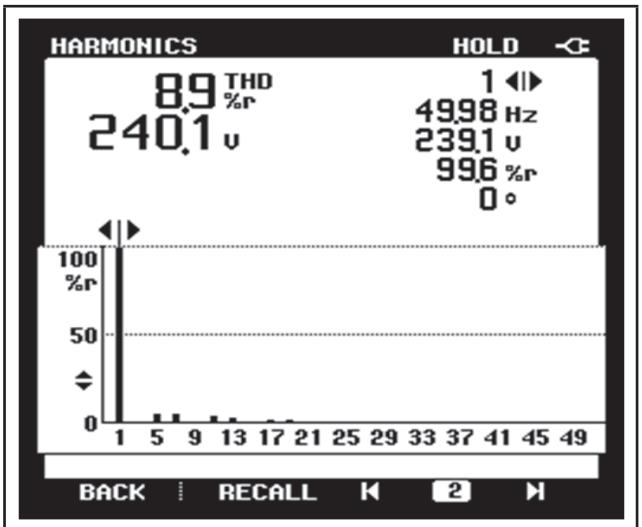

FIG.14 (A)SOURCE VOLTAGE(VS) HARMONIC SPECTRUM

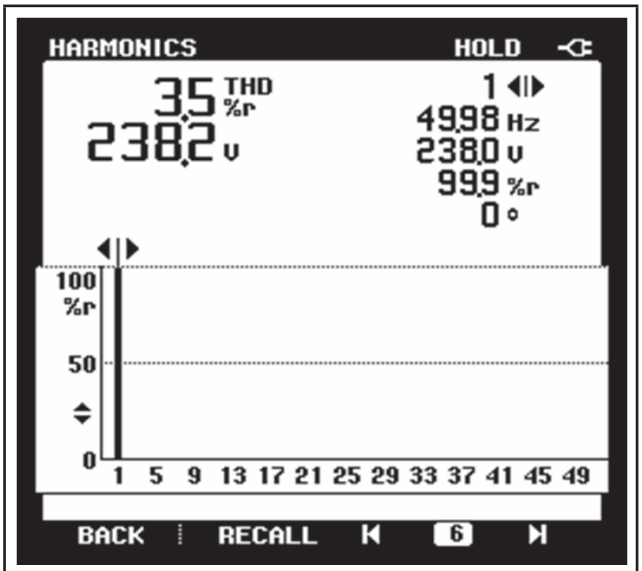

FIG.14 (B) LOAD VOLTAGE (VL) HARMONIC SPECTRUM

APPENDIX

The parameters of Admittance Estimation algorithm based DVR are:

Source voltage: 415 V (L-L), 50 Hz Source Impedance: Rs=0.02 Ω, Ls=2.5 mH Distribution loads: Single phase diode bridge rectifier with R=20 Ω and L=200mH Ripple filter: Rf =5 Ω and Cf =5μF DC bus capacitor Cdc =3000 μF DC voltage PI controller: kdp=1.214, kdp=3.02

PCC voltage PI controller: kqp=4.1, kqp=1.4 AC inductor: 3.00 mH

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